M8050A
High-Performance BERT 120 GBd

Version 5.0

New features:

- Enhanced PCIe 6 link training with two TxEQ change requests
- FEC encoding for 2 and 4 lanes
- Automatic de-emphasis optimization based on TDECQ taps of DCA
- De-emphasis presets and optimization for 200G chip-to-module test

Enabling Your Successful Design Deployments in 800G/1.6T, PCIe and USB4.x

The Keysight M8050A BERT enables success in chip deployments of 800G/1.6T, PCIe, USB4 and other leading technologies by providing an unmatched combination of 120 GBd signaling with uncompromised signal integrity.

KEYSIGHT

Table of Contents

Introduction

The Keysight M8050A high-performance BERT enables accurate characterization of receivers used in next generation data center networks and server interfaces with symbol rates up to 120 GBd.

The M8050A high-performance BERT is one part of the Keysight M8000 Series of BER test solutions. It can be combined with other hardware and software of the M8000 Series.

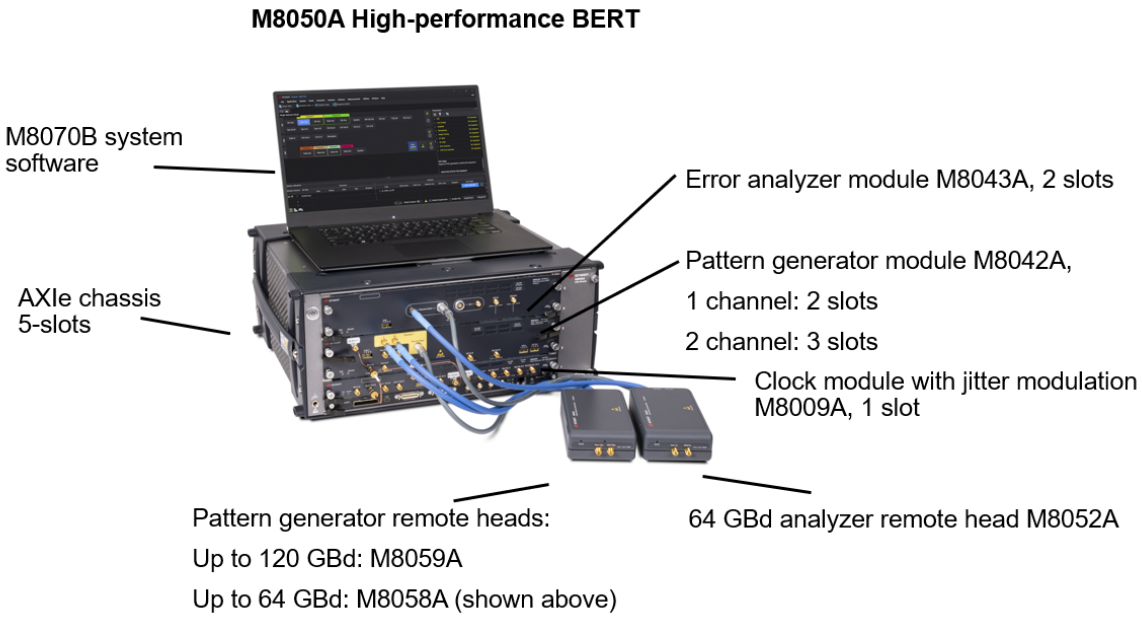

Figure 1. Overview of the M8050A high-performance BERT

Overview of M8050A modules and remote heads covered in this data sheet:

Description	AXIe slots	Product number
120 GBd pattern generator module for one data output channel	2-slot	M8042A-0G1
120 GBd pattern generator module for two data output channels	3-slot	M8042A-0G2
64 GBd remote head with cable connections to M8042A pattern generator module		M8058A
120 GBd remote head with cable connection to M8042A pattern generator module		M8059A
64 GBd high-voltage remote head with cable connections to M8042A pattern generator module		M8068A
120 GBd high-voltage remote head with cable connection to M8042A pattern generator module		M8069A
64 GBd error analyzer module	2-slot	M8043A
58 GBd error analyzer module	1-slot	M8046A
64 GBd analyzer remote head with cable connection to M8043A error analyzer module		M8052A

Specifications for Pattern Generator Module M8042A and Remote Heads M8058A, M8059A, M8068A and M8069A

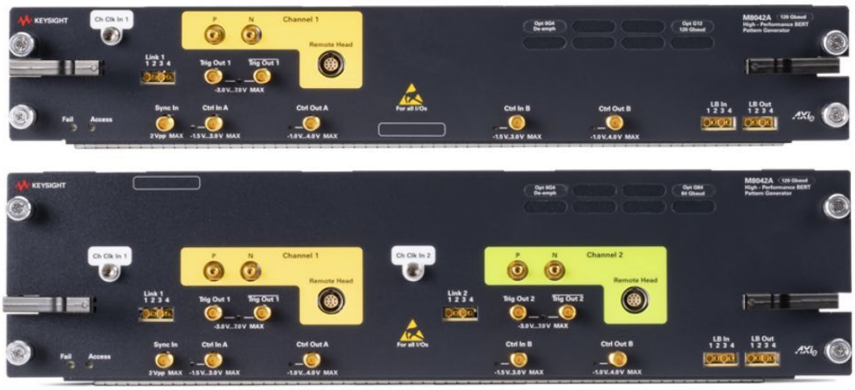

Figure 2. The pattern generator module M8042A is available as one-channel and two-channel version. The one-channel version M8042A-0G1 occupies 2 slots in the AXIe chassis, the two-channel version M8042A-0G2 occupies 3 slots.

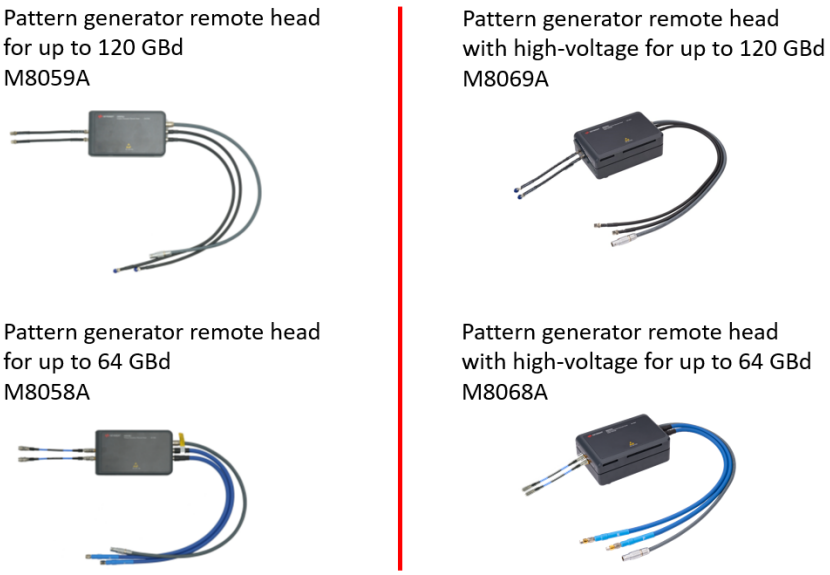

Figure 3. Four remote heads are available for the pattern generator module M8042A. At the top the 120 GBd remote heads M8059A and M8069A are shown with 1.0 mm connectors to accommodate close connection to the device under test for symbol rates up to 120 GBd. The 64 GBd remote heads M8058A and M8068A are shown at the bottom, these provide 1.85 mm connectors. The three cables on the back side of the remote heads are used to connect with the M8042A pattern generator module and are not removable.

The M8042A pattern generator module operates from 2 to 120 GBd. It is available as one-channel or two-channel version. You can select three symbol rate ranges. The M8042A requires a clock module with jitter modulation M8009A, and one remote head for each data output channel. For operations above 64 GBd, the 120 GBd pattern generator remote head M8059A or M8069A is required. Using the P and N output of the M8042A module is prohibited. One M8009A clock generator module is required for each M8042A pattern generator module.

For the following generator functions these module options are required:

- Pattern generation up to 32 GBd for NRZ and PAM4 (M8042A-G32)
- Pattern generation up to 64 GBd for NRZ and PAM4 (M8042A-G64)
- Pattern generation up to 120 GBd for NRZ and PAM4 (M8042A-G12)
- One channel (M8042A-0G1)
- Two channels (M8042A-0G2)
- De-emphasis, module-wide license (M8042A-0G4)
- PAM3 encoding for USB4v2 interfaces (M8042A-0P3)
- PAM6 encoding for 224 Gbps interfaces (M8042A-0P6)
- PAM8 encoding for 224 Gbps interfaces (M8042A-0P8)
- FEC encoding (M8042A-0G9)

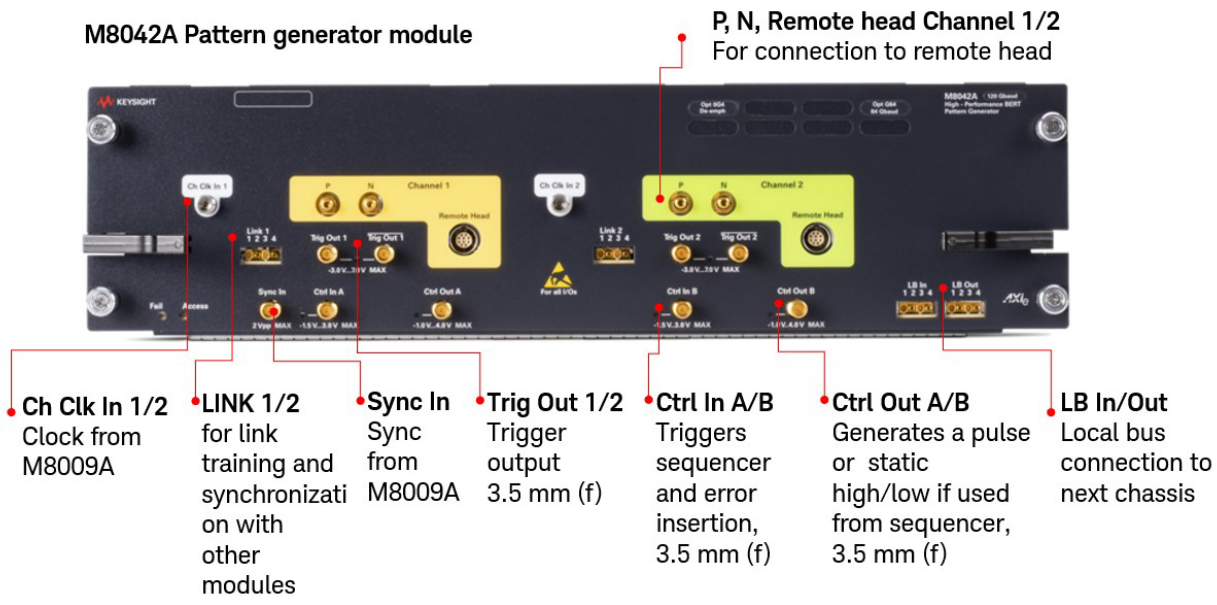

Figure 4. The M8042A pattern generator module provides many supplementary inputs and outputs. Shown here is the overview of all inputs and outputs for a two-channel version of M8042A.

Data Output (Data Out 1, Data Out 2)

Table 1. Data output characteristics for M8042A with M8058A/M8059A and high-voltage remote heads M8068A/M8069A. Values apply at the end of the reference cable at the outputs of the remote heads M8058A, M8059A, M8068A and M8069A.

Parameter	with M8059A/ M8058A remote heads	with M8069A/ M8068A high-voltage remote heads
Symbol rate	2.000 to 120.0 GBd for M8042A-G12 (only with M8059A or M8069A) 2.000 to 64.8 GBd for M8042A-G64 2.000 to 32.4 GBd for M8042-G32 Applies for NRZ and PAM4	
Data formats	NRZ, PAM4 PAM3 (requires M8042A-0P3/UP3) PAM6 (requires M8042A-0P6/UP6). The maximum supported symbol rate is 96 GBd, over-programming is possible. PAM8 (requires M8042A-0P8/UP8). The maximum supported symbol rate is 80 GBd, over-programming is possible.	
Channels per module	1 channel, 2 slots (option 0G1) 2 channels, 3 slots (option 0G2)	
Amplitude	**M8059A:** 100 mVpp to 1.6 Vpp differential 50 mVpp to 0.8 Vpp single ended	**M8069A:** 1 Vpp to 3.6 Vpp up to 113.5 Gbd differential 500 mVpp to 1.8 Vpp up to 113.5 GBd single ended 1 Vpp to 3.4 Vpp from >113.5 to 116 Gbd differential 500 mVpp to 1.7 Vpp from > 113.5 to 116 GBd single ended
	M8058A: 100 mVpp to 1.8 Vpp differential 50 mVpp to 0.9 Vpp single ended	**M8068A:** 1 Vpp to 5 Vpp differential 500 mVpp to 2.5 Vpp single ended
Amplitude resolution	1 mV	3 mV
Amplitude accuracy	±10% ±10 mV typical (AC) [1]	±10% ±30 mV typical (AC) [1]
Symbol level resolution	PAM levels are adjustable in 0.1% steps of amplitude	
Coupling	DC/AC selectable coupling	AC coupling
Output voltage window	–1 to +3.0 V depends on external termination voltage [2]	Not applicable
Common mode voltage accuracy	25 mV ± 12.5% [5]	Not applicable
External termination voltage	–1 to +3.0 V	
Termination modes	Balanced and unbalanced	Not applicable
Termination impedance range	To protect the output stage, the output is disabled when an unexpected voltage or termination impedance is detected. DC output coupling mode: Termination range for devices connected to data out:	Not applicable

	• Unbalanced 50 Ω +15 Ω / –10 Ω • Typical balanced 100 Ω ±30 Ω typical Operation into open is possible for following ranges when DC coupled and balanced termination modes are selected and M8042A module driver Output amplitude max. 450 mV • Offset 0 to 370 mV	
Transition time (20 to 80 %)	**M8059A:** 4 ps typical at 120 GBd 6.5 ps typical at 64 GBd 8 ps typical at 8 GBd **M8058A:** 7 ps typical at 64 GBd 8.5 ps typical at 8 GBd	**M8069A:** 4.5 ps typical at 120 GBd 7.5 ps typical at 64 GBd 11 ps typical at 8 GBd **M8068A:** 6.5 ps typical at 64 GBd 9 ps typical at 32 GBd 10 ps typical at 8 GBd
Intrinsic total jitter [6]	**For M8009A with option -062:** 3.3 ps typical 6 ps typical from 2 to 20 GBd **For M8009A with option -061:** 3.3 ps typical in combination with M8009A-061 7 ps typical from 70 to 80 GBd 6 ps typical from 16 to 33 GBd 7 ps typical from 10 to 16 GBd 9 ps typical from 2 to 10 GBd	
Intrinsic random jitter [6] (NRZ)	**For M8009A with option -062:** 7 mUI rms typical from 2 to 40 Gbd 10 mUI rms typical from 40 to 110 GBd 12 mUI rms typical for > 110 GBd **For M8009A with option -061:** 10 mUI rms typical 15 mUI rms typical from 105 to 120 GBd 20 mUI rms typical from 99 to <105 GBd 40 mUI rms typical from 70 to 80 GBd 15 mUI rms typical from 30 to 33 GBd 7 mUI rms typical from 24 to 30 GBd	
Clock/2 jitter range	±50 mUI or ±4 ps typical (whatever is less) for symbol rates above 7.9 GBd. Note: this means that first eye can be up to 50 mUI or 4 ps longer or shorter than subsequent eye	
Adjustable clock/2	For each channel independently	
SNDR [3] with randomizer off	**M8059A:** 53.125 GBd: 35 dB typical 106.25 GBd: 31 dB typical **M8058A:** 53 to 58 GBd: 35 dB typical	**M8069A:** 53.125 GBd: 32 dB typical 106.25 GBd: 28 dB typical **M8068A:** 53 to 58 GBd: 35 dB typical
SNDR [3] with randomizer on	**M8059A:** 53.125 GBd: 35 dB typical 106.25 GBd: 32.5 dB typical **M8058A:** 53 to 58 GBd: 35 dB typical	**M8069A:** 53.125 GBd: 32 dB typical 106.25 GBd: 28 dB typical **M8068A:** 53 to 58 GBd: 35 dB typical
Level random noise	**M8059A:** 53.125 GBd: 4.75 mV rms differential typical	**M8069A:** 53.125 GBd: 14 mV rms differential typical

	106.25 GBd: 6 mV rms differential typical **M8058A:** 53 to 58 GBd 5.5 mV rms differential typical	106.25 GBd: 20 mV rms differential typical **M8068A:** 53 to 58 GBd: 16 mV rms differential typical
Data delay	Delay range 100 ns Delay accuracy: ± (maximum (1.5 ps or 25 mUI whatever is higher) + 1% of entered value) typical	
Skew between normal and complement	2 ps maximum at the end of the reference cable pair. Fixed. 1 ps maximum at connector of remote head Reference cable pair M8059A-801 and M8058A-801 has 1 ps	
Skew between data output ch 1 and ch 2 in one M8042A module	Repeatability: < 1 ps typical Absolute skew: < 10 ps measured	
Skew between data outputs of two M8042A modules	Repeatability: < 15 ps typical Absolute skew: < 15 ps measured	
Electrical idle, (squelch)	The output transitions from full swing to 0 V amplitude and vice versa at constant offset within 1 UI. Normal and complement output have same level (Max – Min)/2	
Squelch granularity	Pattern Editor (NRZ only): bit granularity When controlled from sequencer: sequencer block wise	
Automatic eye performance optimization by using an external oscilloscope	Yes, requires M8070ADVB.	
Connectors at data output of M8042A	1.0 mm, female	
Connectors at data output of remote head	**M8059A, M8069A:** 1.0 mm, female	**M8058A, M8068A:** 1.85 mm, female
Reference cables	**M8059A:** Matched cable pair 1.0 mm (m) to 1.0mm (m), 150 mm, 1 ps M8059A-801. (Keysight part number M8059-61621) **M8058A:** Matched cable pair 1.85 mm (m) to 1.85 mm (m), 150 mm, 1 ps M8058A-801. (Keysight part number M8199-61610)	**M8069A:** Matched cable pair 1.0 mm (m) to 1.0mm (m), 150 mm, 1 ps M8059A-801. (Keysight part number M8059-61621) **M8068A:** Matched cable pair 1.85 mm (m) to 1.85 mm (m), 150 mm, 1 ps M8058A-801. (Keysight part number M8199-61610)
Recommended attenuators:	n/a	In case you need to protect inputs of an oscilloscope, e.g. DCA module N1046A **For M8069A**: 10 dB attenuator with 1.0 mm connectors: Keysight part number 0955-4009 **For M8068A:** 10 dB attenuator 8490G
Pre-requisites		M8042A module driver 4.5 or higher.

1. At 5 GBd measured with DCA-X N1046A and clock pattern and in the middle of the eye
2. High level voltage range= 2/3* Vterm - 0.95 V < HIL < Vterm + 2 V. Low level voltage range= 2/3 * Vterm - 1 V < LOL < Vterm + 1.95 V
3. Measurement procedure according to section 120D.3.1.6 of IEEE specification
4. Measured at 90% of maximum amplitude
5. Common mode voltage = 0.5 * (measured offset at Normal + measured offset at Complement). Measured with DCA N1046A and 10dB attenuator.
6. Measured with N1060A and PTB signal from Ref clk out 16G from M8009A, NRZ, PRBS15, @ BER 1e-12.

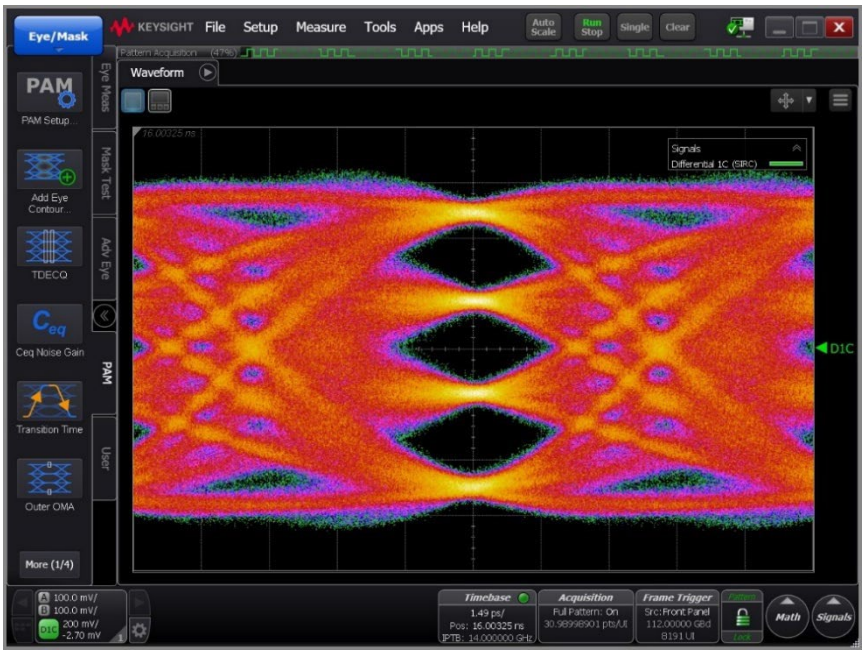

Figure 5. Clean 112 GBd PAM4 output signal of M8042A pattern generator module with remote head M8059A. This uses the clock module M8009A with an internal oscillator. The output amplitude is set to 1.0 Vpp differential and PRBS 2^{15}-1. Measured with DCA-X and N1046A.

De-emphasis

The M8042A provides built-in de-emphasis with positive and negative cursors based on a Finite Impulse Response (FIR). Users can enter the de-emphasis in coefficient values.

Table 2. De-emphasis characteristics for M8042A. Requires Option -0G4

De-emphasis	Range if used as cursor	Range if used as main cursor
De-emphasis taps	7, can be adjusted for each channel independently 1 UI spacing	
Preset table	50 presets editable in xml file	
Cursor (c0)	0.0 to ±0.45 [1]	
Cursor (c1)	0.0 to ±0.45 [1]	
Cursor (c2)	0.0 to ±0.45 [1]	0.3 to 1.0 [1]
Cursor (c3)	0.0 to ±0.45 [1]	0.3 to 1.0 [1]
Cursor (c4)	0.0 to ±0.45 [1]	0.3 to 1.0 [1]
Cursor (c5)	0.0 to ±0.45 [1]	
Cursor (c6)	0.0 to ±0.45 [1]	
Cursor coefficient resolution	0.004 Hardware capable resolution, user interface allows 0.001 steps	
Main cursor	Configurable position between c2 and c4	

1. Sum of all cursors absolute values may not exceed 1.0. Each absolute value of a cursor must be < as value of main cursor.

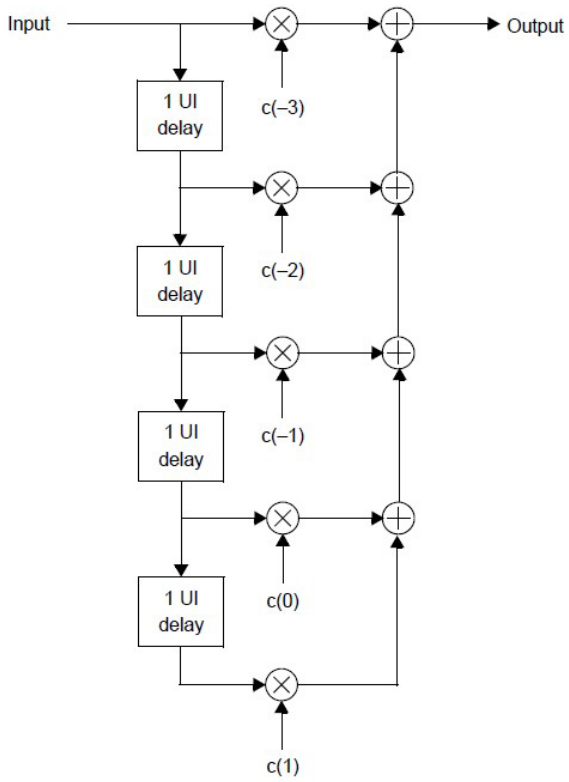

Figure 6. The pattern generator provides built-in de-emphasis to emulate a TX equalizer. The example shows a configuration for IEEE802.3 ck with three pre-cursors c(-3), c(-2) and c(-1), the main cursor c(0), and one post cursor c(1).

De-emphasis presets for PCIe testing

If PHY protocol mode PCIe3, PCIe4, PCIe5, PCIe6 for the pattern generator sequence is selected the de-emphasis capabilities are switched from the multi-tap FIR to a PCI Express type of FIR editor with coefficient entry as integers dependent of the selected full swing. A full swing from 24 to 63 coefficient resolution steps can be selected.

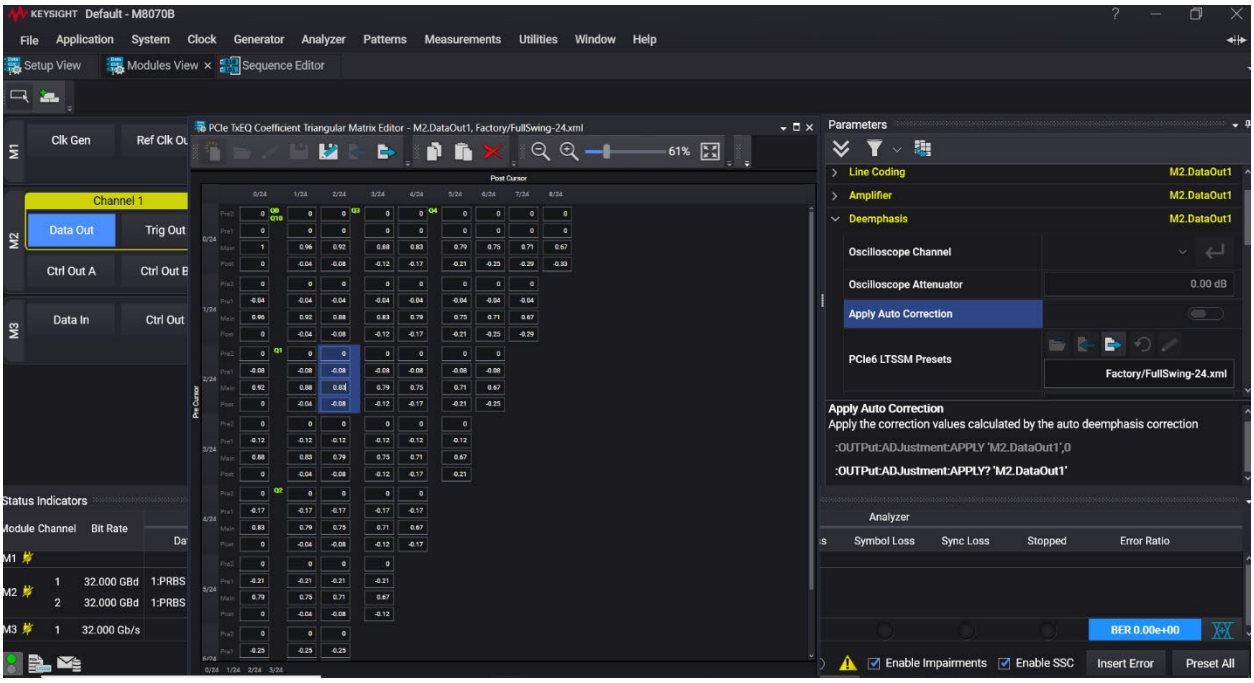

Figure 7. The TxEQ matrix editor can be accessed if the PHY protocol mode PCIe 3, PCIe 4 or PCIe 5 is selected for the pattern generator sequence.

Forward Error Correction (FEC) encoding

The M8042A pattern generator module supports Forward Error Correction (FEC) and precoding encoding according to IEEE802.3cd.

Users can inject pre- and post-FEC errors to test the device's FEC decoder function.

Table 3. Specifications for FEC (Forward Error Correction) encoding. Requires M8042A option -0G9.

FEC encoding	100GBASE-R, 200GBase-KP4, 2x400GBase-KP4
Reed-Solomon code	RS (544,514)
Scrambler	PRBS 2^{58}-1
Pattern sequence	These patterns from pattern library can be FEC encoded: Remote faults, Scrambled idle
Line coding	PAM4
Symbol rate	53.125 GBd PAM4: 100GBASE (all PCS lanes), 200GBASE and 2x400GE (PCS 0→3 on PG1 and PCS 4→ 7 on PG2)
FEC symbol error injection	No FEC error insertion
Pre-coder	PAM4: 1/ (1+D) mod4, can be switched on/off. Follows IEEE802.3 Clause 135.5.7.2. for PAM4 encoded lanes.
Pre-requisites	M8042A with option 0G9

USB4 LFPS Generator

The USB4 LFPS Generator utility generates LFPS patterns with the M8070B software, allowing configuration of cycles, period, duty cycle, pre-data, and idle duration. Supported by M8042A and

M8045A modules, it handles USB4 Gen 2 (10 Gbps), Gen 3 (20 Gbps), and Gen 4 (25.6 GBd) data rates. The LFPS Generator offers Calibration and Rx testing modes, controllable with Start and Stop buttons.

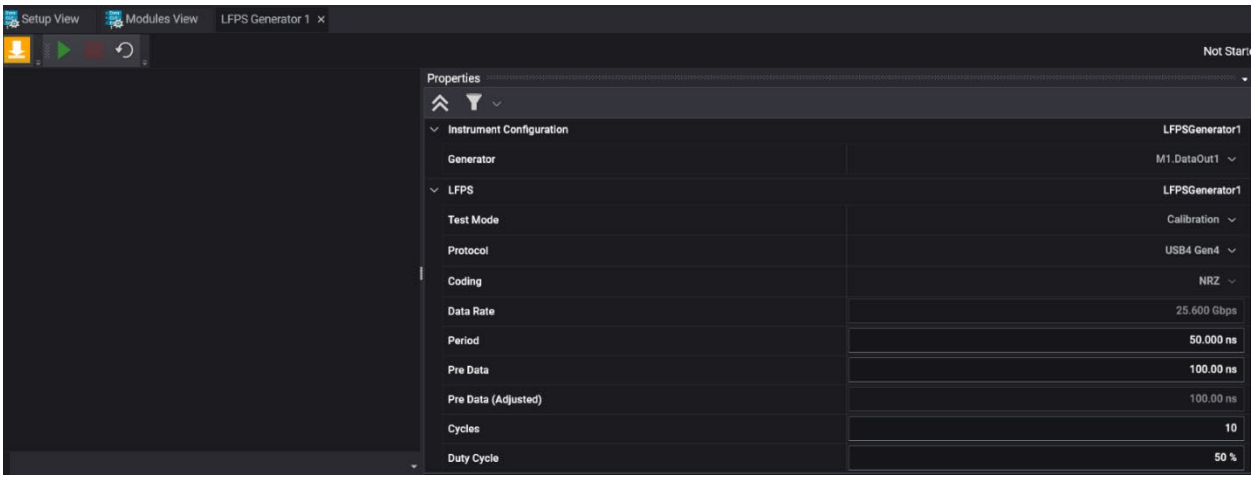

Figure 8. The USB4 LFPS generator utility

Trigger output 1/2 (Trig Out 1, Trig Out 2)

The trigger output can be used in different modes:

- Divided clock with dividers:
  - Max output frequency is 8.0 GHz, divider range 2 to 65000
  - Minimum divider n is the next integer value above the symbol rate/ 8 GHz
  - (Example: for a symbol rate of 53 GBd, n = 7, because it is the next higher integer of 53 / 8 = 6.625)
- Sequence block trigger
- Pulse mode triggered by sequencer (only if memory pattern is used)
  - Pulse width min 16 UI. Max block length
  - Offset min 0. Offset Max block length -1
- “Pulse on PRBS” mode (NRZ only). Matched pattern without ignoring defined bits (only if algorithmic pattern is used)
  - Pulse width: minimum 16 UI, maximum PRBS length.

The trigger output 2 is only available for the two-channel version of M8042A.

Table 4. Trigger output characteristics of M8042A

Parameter	
Amplitude	0.1 to 1.0 Vpp single ended
Jitter injection	The injected jitter is always the same as the jitter at the Data Out (excluding clk/2)
Delay	Follows Data Out delay Relative Trigger to Data Out delay: Range: 0 to 1000 UI with 1 UI resolution
Skew between trigger output and data output of same channel	460 ps maximum (measured)
Output voltage window	–1 to 3 V 1
External termination voltage	–1 to 3 V
Interface	50 Ω
Connector	3.5 mm, female

1. High level voltage range= 2/3*Vterm – 0.9 V < HIL < Vterm + 2 V
   Low level voltage range= 2/3 *Vterm – 1 V < LOL < Vterm + 1.9 V

Control input A/B (Ctrl In A, Ctrl In B)

Each control input can be selected as: sequence trigger, error insertion.

Table 5. Control input characteristics

Parameter	
Input voltage	–1 V to +3 V
Termination voltage	–1 V to +3 V
Termination voltage accuracy	± (25 mV +1%)
Threshold voltage	–1 V to +3 V
Delay repeatability to data output	±512 UI maximum
Absolute delay to data output	< 25 µs
Connector	3.5 mm, female

Control output A/B (CTRL Out A, CTRL Out B)

This output provides a pulse or static high/low if used from sequencer.

Table 6. Control output A/B characteristics

Parameter	
Amplitude [1]	0.1 to 2 V
Output voltage window [1]	–0.5 to 1.75 V
Delay to data output	±512 UI maximum
Connector	3.5 mm, female

1. When terminated with 50 Ω into GND. Doubles into open.

LINK 1/2 (Link1, Link 2)

LINK 2 is only available for the two-channel version of M8042A.

This communication link enables interactive link training with low latency between a pattern generator channel and a M8046A analyzer module. Requires cable M8051A-801.

Channel clock input 1/2 (Ch Clk In 1/2)

The channel clock inputs are used to connect with the M8009A clock module.

The channel clock input 2 is only available for the two-channel version of M8042A.

Connector: 1.85 mm, female

These are the supported cables to connect M8042A with M8009A:

M8042A-801: Clock cable semi-rigid for M8042A channel 1 (part number M8042-61621)

M8042A-802: Clock cable semi-rigid for M8042A channel 2 (part number M8042-61622)

Alternatively, to the semi-rigid clock cable, the 450 mm clock cable 1.85 mm (m) to 1.85mm (m) can be used. Its orderable as M8199A-810 (part number M8199-61624, included in M8042A-810 cable kit)

Synchronization input (Sync In)

The synchronization input is used to connect with M8009A clock module.

Connector: 3.5 mm, female

This is the supported cable to connect M8042A with M8009A:

M8042A-801: Synchronization cable, 3.5 mm, semi-rigid for M8042A and M8009A (part number M8042-61623)

Local bus input/output (LB In, LB Out)

The local bus input is needed for communication connected to the previous AXIe chassis.

The local bus output is needed for communication connected to the next AXIe chassis.

The connection cable is a 4-wire mini coax cable M8051A-801 (part number M8041-61601)

Pattern and Sequencing

Table 7. Specifications for patterns and sequencing for pattern generator and error analyzer

Parameter	Pattern generator M8042A	Error analyzer M8043A
PRBS	2^n-1, n= 7, 10, 11, 15, 23, 23p, 31, 33, 35, 39, 45, 49, 51	Yes, same as M8042A
PRBS	2^n, n=7, 10, 11, 13, 15	Yes, same as M8042A
QPRBS	OIF-CEI: QPRBS13-CEI, QPRBS31-CEI IEEE 802.3: QPRBS13, PRBS13Q, PRBS31Q	Yes, same as M8042A
PRTS	3^n-1, n=17, 19, 23	No. For PAM3 support please check M8046A
User definable pattern memory	NRZ: 2 Gbit/ channel PAM3 and PAM4: 1 Gsymbol/ channel PAM6 and PAM8: 1 Gsymbol/ channel	Yes, same as M8042A
Pattern	Export, import. Or factory patterns provided by M8070B	Yes, same as M8042A
Mark density	PRBS 1/8 to 7/8	
PAM4 coding	Gray coding Uncoded Custom mapping of 00, 01,10,11 to symbols 0, 1, 2, 3.	Yes, same as M8042A
Pre-coder	Yes (only for NRZ and PAM4)	No
PAM3 coding	Uncoded Custom mapping of 00, 01,10, to symbols 0, 1, 2. 11 is interpreted as symbol 0. Memory based patterns only	No. Please check M8046A
PAM6 coding	Uncoded Custom mapping of 000, 001,010,011,100,101 to symbols 0, 1, 2, 3, 4, 5. 110 and 111 are interpreted as symbol 0. Editable XML file allows to map 5 bits to 2 symbols and 3 bits to 1 symbol. Memory based patterns only.	No. Please check UXR based error analysis.
PAM8 coding	Uncoded Custom mapping of 000, 001,010,011,100,101,110, 111 to symbols 0, 1, 2, 3, 4, 5, 6, 7. Editable XML file allows to map 5 bits to 2 symbols and 3 bits to 1 symbol. Memory based patterns only	No. Please check UXR based error analysis.
Scrambler	PAM3 only (according to USB4v2)	No
Vector/ sequencer granularity	NRZ: 512 bit, PAM3/4/6/8: 256 Symbols	Yes, same as M8042A
Pattern capture for M8043A	n/a	Yes, raw data • Capture data starts on event

		• User defined (minimum) amount of pre-event bits/ symbols and minimum capture bit/symbols • Events: single error, user-defined error bursts, CTRL In, immediate • Max 2 Gbit/ch capture data for NRZ, 1 Gsymbol / ch for PAM4 Save captured data: • With errors • As expected, data (ignores error content) • As PG data (ignores error content) • Export via pattern editor windows • Convert bits into all other codings and vice versa • Ability to mask error bits automatically. Display of captured data: • Display errors with color coding • Navigate through error bits/symbols (find next/previous)
Pattern sequencer	3 counted loop levels, 1 infinite loop, # of blocks: 500 Minimum block length NRZ: 2048 Bits Minimum block length PAM3/4/6/8: 1024 Symbols	Same as M8042A for PAM3, PAM6, PAM8.
Error insertion	NRZ, PAM3/4/6/8: Single symbols, ratio variable/ fixed. [1] Error ratio range For PAM3: 10^n (n= -4 to -12) For NRZ/PAM4/8: 10^n (n= -1 to -12) resulting SER For PAM3/4: 2 times set error ratio. For PAM6/8: 3 times set error ratio. Error insertion trigger: Manual, CTRL IN and sequencer break	n/a
Masking	n/a	Expected bits can be masked (ignored) during error counting. Bitwise and block-wise masking is possible.

1. For PAM6 resulting BER and SER does not match with set value. For PAM3 BER is around 1.33 times of set error ratio

Specifications for Clock Module with Jitter Modulation M8009A

Figure 7. The M8009A-062 clock module with jitter modulation is a 1-slot AXIe module. The M8009A clock module with option -061 has the same connectors, except that there is no Clk Out 32G.

The M8009A clock module with integrated jitter modulation operates from 4 to 60 GHz. It can be locked to external reference clocks.

For the following functions a module option is required:

Advanced jitter modulation for up to two channels, license (M8009A-0G3)

Reference clock multiplier, license (M8009A-0G6)

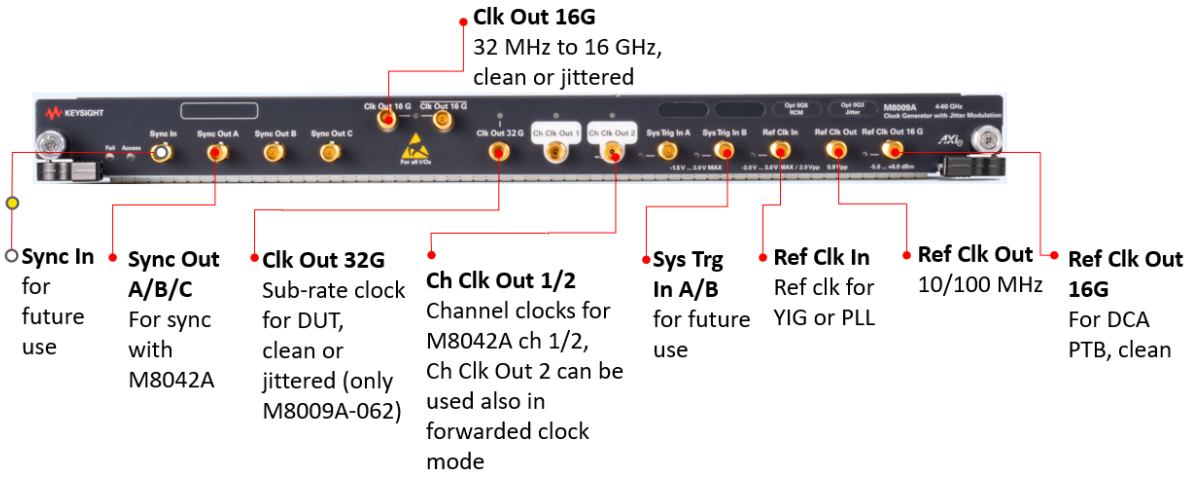

Figure 8. This figure gives an overview of all inputs and outputs of the M8009A-062 clock module with jitter modulation.

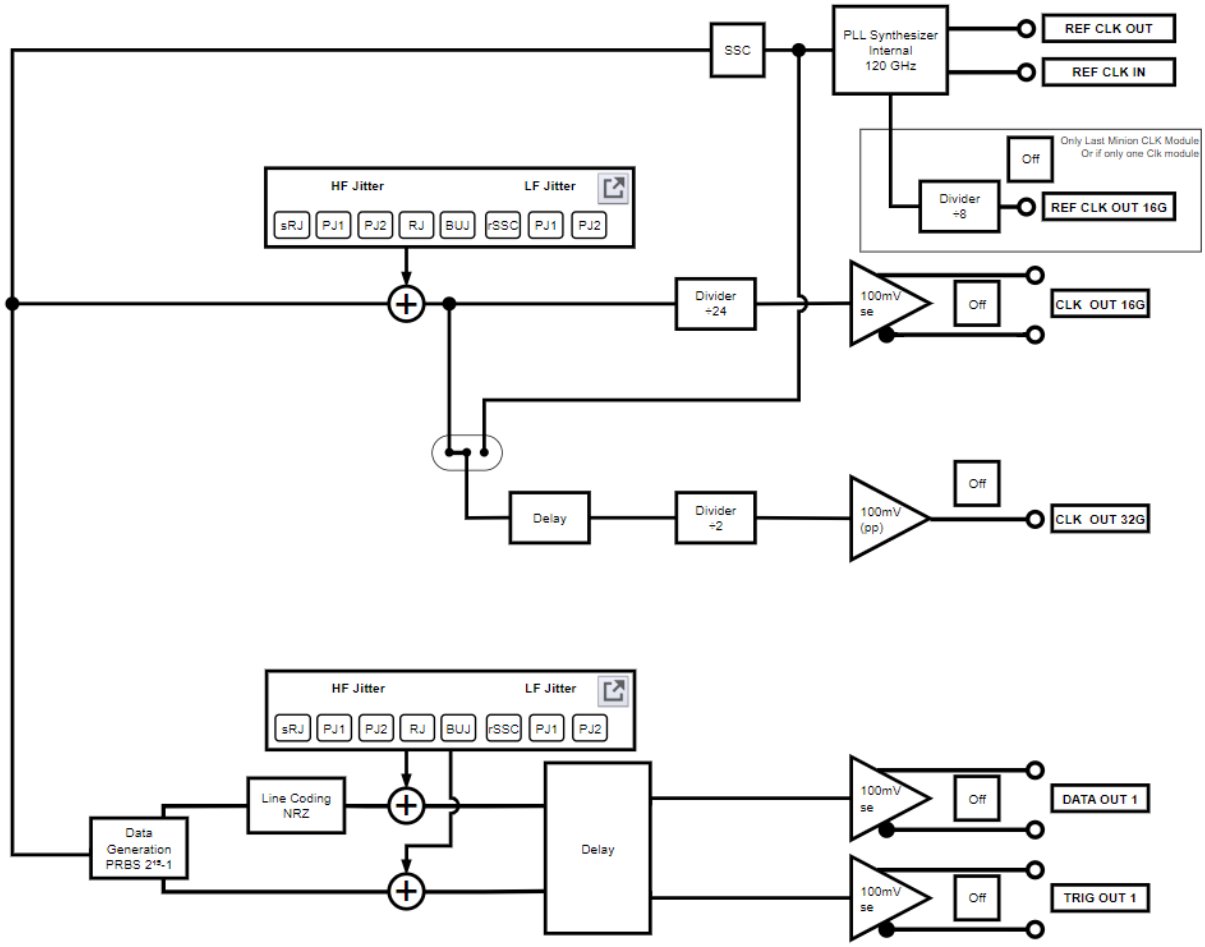

Figure 9. Simplified block diagram of the M8009A-062 clock module with jitter modulation and M8042A pattern generator module. Shown is a one channel configuration.

Internal Synthesizer and Clock Modes for M8009A

Table 8. Internal synthesizer characteristics of M8009A

Parameter	
Frequency accuracy	±2 ppm
Frequency resolution	1 Hz

Table 9. Clock modes for M8009A

Clock mode	Clock generation	Input frequency range
Internal	PLL with internal reference	N/A
Reference clock	PLL with bandwidth < 100 kHz	10 or 100 MHz
Direct clock	No PLL. Maximum output frequency is 60 GHz	8 to 16.2 GHz
Reference clock with multiplier bandwidth	Multiplying PLL with m/n PLL with loop bandwidth: 100 kHz, others: see table 13, m, n = 1 to 12000	10 MHz to 16.2 GHz

Channel clock output 1 (Ch Clk Out 1)

This signal provides the clock signal for the pattern generator M8042A and AWG modules. Ch Clk Out 1 has to be connected to Ch Clk In 1 of the M8042A module.

Table 10. Channel clock output characteristics.

Parameter	
Frequency range	4.0 to 60 GHz
Channels per module	1
Amplitude	Automatically adjusted for M8042A clock inputs
Frequency resolution	1 Hz
Frequency accuracy	±2 ppm typical (internal reference)
Data delay range	see M8042A
Intrinsic random jitter	For M8009A module with option -062: 3.5 mUI rms typical up to 20 GHz 5 mUI rms typical > 20 GHz 6 mUI rms typical > 55 GHz For M8009A modules with option -061 the following applies: 10 mUI rms typical @ 58 GHz 6 mUI rms typical @ 32 GHz 8 mUI rms typical @ 16 GHz Refers to mUI of Ch Clk Out 1 frequency
Termination	50 Ω into GND. Do not operate into open. Unused outputs must be terminated
Coupling	AC
Connectors	1.85 mm, female

Channel clock output 2 (Ch Clk Out 2)

This output can be switched between two modes:

Channel clock mode

- This signal provides the clock signal for the second channel of the pattern generator M8042A. Ch Clk Out 2 has to be connected to Ch Clk In 2 of the M8042A module. Independent jitter profile for Ch Clk Out 2 compared to Ch Clk Out 1

Forwarded clock mode

- This signal is intended to be used to drive a DUT that requires a data rate divide by a second clock. It can contain identical jitter as the Ch Clk 1 Output 1. This clock signal is synchronous to the data pattern, phase relation will change when divider settings are modified.

Table 11. Channel Clock Output 2 characteristics in Channel Clock Mode

Parameter	Forwarded clock mode	PG module clock mode
For M8009A modules with option -062 the following applies:		
Frequency range	4 to 60 GHz	4 to 60 GHz
Frequency divider factors	Symbol rate / clock divider is fix, value 2	NA
Intrinsic random jitter	3.5 mUI rms typical up to 20 GHz 5 mUI rms typical > 20 GHz	3.5 mUI rms typical up to 20 GHz 5 mUI rms typical > 20 GHz
For M8009A modules with option -061 the following applies:		
Frequency range	2 to 32.4 GHz	4 to 32.4 GHz
Frequency divider factors	Symbol rate / clock divider n with n = 2, 4, 8, 16, 32	NA
Intrinsic random jitter	10 mUI rms typical @ 16 and @ 32 GHz. Refers to mUI of Ch Clk Out 1 frequency	6 mUI rms typical @ 32 GHz 8 mUI rms typical @ 16 GHz Refers to mUI of Ch Clk Out 1 frequency
The following specifications are valid for M8009A-061 and -062:		
Amplitude	0.5 to 1.2 Vpp typical, single ended	Automatically adjusted
Duty cycle	50%, Accuracy ± 10% typical	50%, Accuracy ± 10% typical
Data delay range	NA	See M8042A
Jitter delay range	±40 ns	±40 ns
Termination	50 Ω into GND. Do not operate into open.	50 Ω into GND. Do not operate into open.
Coupling	DC, use DC-blocks when non-GND termination voltages are present." also applies to this output	n/a
Connectors	1.85 mm, female	1.85 mm, female

Clock output 32G (Clk Out 32 G)

This signal is intended to be used to drive a DUT that requires a sub-rate clock. It can contain identical jitter as channel clock output 1. The clock signal is aligned to the data pattern. Its only available on M8009A modules with Option -062.

Table 12. Clock output 32 G characteristics (available on M8009A-062)

Parameter	
Frequency range	1 to 32.4 GHz
Frequency divider factors	Symbol rate / clock divider n with n = 2, 4, 8, 16, 32
Amplitude	Adjustable from 0.5 to 1.2 Vpp typical, single ended
Duty cycle	50%, Accuracy ± 10% typical
Jitter source	Clean clock: no SSC, no jitter Follow Clk out 16G: jitter has same profile as Clk Out 16G
Intrinsic random jitter	3 mUI rms typical. Refers to mUI of Ch Clk Out 1 frequency
Delay range	0 to 100 ns relative to Ch Clk Out 1
Delay accuracy	± (maximum (1.5 ps or 25 mUI whatever is higher) + 1% of entered value) typical
Jitter delay range	±40 ns
Termination	50 Ω into GND. Do not operate into open.
Coupling	DC, use DC-blocks when non-GND termination voltages are present.
Connectors	1.85 mm, female

Reference clock input (Ref Clk In)

This input allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator.

Table 13. Reference clock input characteristics

Parameter	
Input amplitude	0.2 to 2.0 Vpp
Input frequency	
Reference mode	10 MHz or 100 MHz (±1%), sinewave or square wave
Direct mode	8 GHz to 16.2 GHz, Sinewave or square wave, input amplitude should be 1.0 to 1.2 Vpp
Clock multiplier mode	10 MHz to 16.2 GHz, sine wave or square wave
Termination	Single ended, 50 Ω, AC coupled
Connector	3.5 mm, female

Table 14. Reference clock multiplier characteristics. Requires M8009A-0G6

Ref clock input	Standard	Target symbol rate	Multiplier/divider	PLL loop bandwidth
100 MHz	PCIe	32 GBd PAM4	320	2 MHz
100 MHz	PCIe	16/ 32 Gb/s NRZ	160/ 320	2 MHz
100 MHz	PCIe	2.5/ 5.0/ 8.0 Gb/s NRZ	25/ 50/ 80	5 MHz
100 MHz	USB4 Gen 2 and 3	10/ 20 Gb/s NRZ	100/ 200	5 MHz
103.125 MHz	TBT3 Gen 2	10.3125 Gb/s NRZ	100	5 MHz
103.125 MHz	TBT3 Gen 3	20.625 Gb/s NRZ	200	5 MHz
19.2 MHz [1]	MIPI M-PHY	2.496/ 2.9184/ 4.992/ 5.8368/ 9.984/ 11.6736 Gb/s NRZ	130/ 152/ 260/ 304/ 520/ 608	2 MHz
26 MHz [1]	MIPI M-PHY	2.496/ 2.912/ 4.992/ 5.824/ 9.984/ 11.648 / 19.968/ 23.296 Gb/s NRZ	96/ 112/ 192/ 224/ 384/ 448/ 768/ 896	2 MHz
38.4 MHz [1]	MIPI M-PHY	2.496/ 2.9184/ 4.992/ 5.8368/ 9.984/ 11.6736/ 19.968/ 23.3472 Gb/s NRZ	65/ 76/ 130/ 152/ 260/ 304 /520/ 608	2 MHz
52 MHz [1]	MIPI M-PHY	2.496/ 2.912/ 4.992/ 5.824 9.984/ 11.648/ 19.968/ 23.296 Gb/s NRZ	48/ 56/ 96/ 112/ 192/ 224/ 384/ 448	2 MHz

1. These reference clock multipliers are supported for M8009A-062 only.

Reference clock output (Ref Clk Out)

This signal provides a reference clock to lock with other instruments in the test setup.

Table 15. Reference clock output characteristics

Parameter	
CLK frequencies	10 MHz or 100 MHz (100 MHz is not available when using external 10 MHz Ref Clk In). Note: always derived from selected clock source, except in direct & clock multiplier mode. Then Ref Clk Out is derived from internal oscillator.
Amplitude	900 mVpp typical single ended into 50 Ω, AC coupled square wave
Termination	50 Ω, nominal
Connector	3.5 mm, female

Reference clock output 16G (Ref Clk Out 16G)

This signal provides a clock between 8 and 16 GHz, relative to symbol rate.
It can be used as clock input or as trigger input for a precision time base of a DCA. Clean clock only.

Table 16. Reference clock output 16G characteristics

Parameter	
CLK frequency range	8 to 16.2 GHz
Amplitude	1100 mVpp sinusoidal typical, AC coupled
Intrinsic random jitter	150 fs rms typical
Termination	50 Ω, nominal
Termination voltage range	±500 mV nominal
Connector	3.5 mm, female

Clock output 16G (Clk Out 16G)

This signal provides a reference clock for a DUT. It can be operated with jitter and without jitter. It provides a differential clock with adjustable amplitude, offset and termination. No phase alignment to data output.

Table 17. Clock output 16G characteristics

Parameter	
Frequency range	31.25 MHz to 16.2499 GHz
Frequency divider factors	n * (1,2,3, to 256) n = 2, 4, 8
Amplitude	0.2 Vpp to 1 Vpp single ended into 50 Ω
Voltage window	-1.0 V to 3.7 V into 50 Ω
Duty cycle	50%, accuracy ±10% typical < 10GHz 50%, accuracy ±15%, typical 10GHz to 16.2499GHz
Intrinsic random jitter	350 fs rms typical clock divider = 1
Jitter injection	LF jitter • Can be set independently from Data Out • LF jitter parameters and range; same as for Data Out • Requires M8009A option -0G3 • HF jitter • Same values as Data Out 1, individually selectable per jitter type SSC • Same as Data Out
Termination	50 Ω into GND or external termination voltage. Do not operate into open.
Coupling	DC coupled, differential.
Connectors	3.5 mm, female

System trigger input A/B (Sys Trg In A, Sys Trg In B)

This signal is reserved for future use.

Table 18. System trigger input A/B characteristics

Parameter	
Input voltage	–1 V to +3 V
Termination voltage	–1 V to +3 V
Threshold voltage	–1 V to +3 V
Connector	3.5 mm, female

Synchronization input (Sync In)

In a 4-channel configuration this input is used on the secondary M8009A clock module to receive the synchronization signal from the primary M8009A clock module.

4-channel configuration is only supported for M8009A-062.

Table 19. Synchronization input characteristics

Parameter	
Cable required	M8199-61620. It is included in the M8042A-810 cable kit.
Connector	3.5 mm female

Synchronization output A/B/C (Sync Out A, Sync Out B, Sync Out C)

This output is used to transmit the synchronization signal to an M8042A module. In a 4-channel configuration it is also used to transmit the synchronization signal from the primary M8009A clock module to the secondary M8009A clock module.

4-channel configuration is only supported for M8009A-062.

Table 20. Synchronization output A/B/C characteristics

Parameter	
Cable required	M8199-61620 (it is included in the M8042A-810 cable kit)
Amplitude	0.6 Vpp typical square wave into 50 Ohm
Connector	3.5 mm female

Jitter Specifications

The M8009A has integrated and calibrated jitter sources. M8009A Option –0G3 is required.

Low-frequency jitter

Table 21. Specifications for low frequency periodic jitter (requires M8009A-0G3). Values shown are applicable at the data output of pattern generator remote heads M8058A and M8059A.

Parameter	Condition	Range
Amplitude range	For modulation frequencies of 100 Hz to 10 kHz:	0 to 8000 UI see table below.
	For modulation frequencies between 10 kHz and 40 MHz and symbol rate < 3.95 GBd	0 to 20 MUI/s / Fmod
	For modulation frequencies between 10 kHz and 40 MHz and symbol rate between 3.95 and 7.9 GBd	0 to 40 MUI/s / Fmod
	For modulation frequencies between 10 kHz and 40 MHz and symbol rate > 7.9 GBd	0 to 80 MUI/s / Fmod
Frequency range	100 Hz to 40 MHz, sinusoidal modulation	
Jitter amplitude accuracy	±2% ±1 ps typical	
Adjustable	For each data channel independently, same LFPJ for data and trigger. Clk Out 16G can be set independently.	

Table 21. Low frequency periodic jitter ranges.

Symbol rate	Max UI at modulation frequency 100 Hz to 10 kHz	Max UI at modulation frequency 10 MHz	Max UI at modulation frequency 40 MHz
2.0 to 3.95 GBd	2000 UI	2.0 UI	0.5 UI
3.95 to 7.9 GBd	4000 UI	4.0 UI	1 UI
7.9 to 120.00 GBd	8000 UI	8.0 UI	2.0 UI

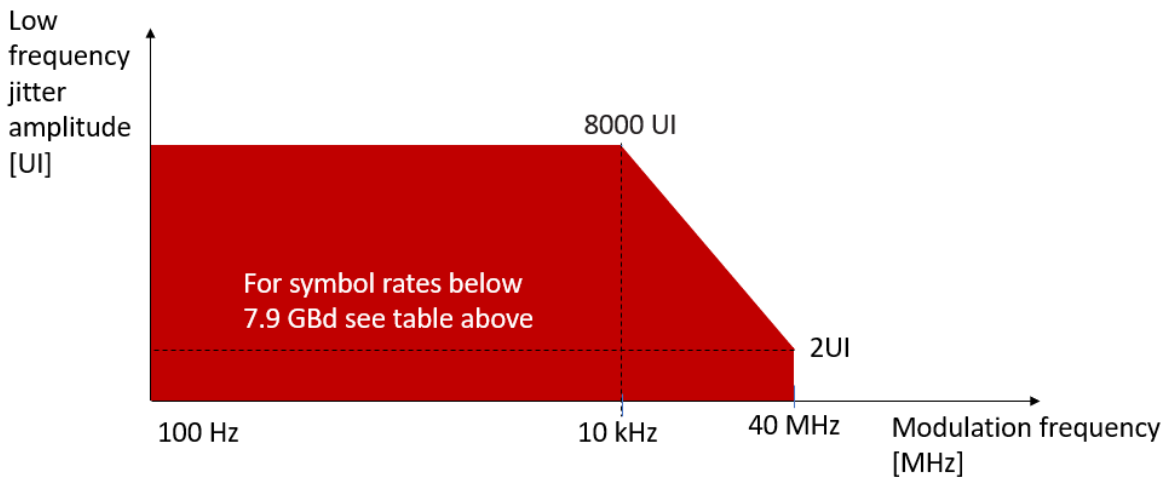

Figure 10. The multi-UI low frequency jitter range depends on selected baud rate and jitter modulation frequency. The graph shows the available range for symbol rates above 7.9 GBd when SSC is disabled.

High-frequency jitter

Table 23. High frequency jitter range (requires M8009A-0G3). This is the maximum sum of RJ, sRJ, HFPJ1, HFPJ2, and BUJ. Values shown are peak-peak and applicable at the data output of pattern generator remote heads M8058A and M8059A.

For symbol rates	Applicable for	Sum
≥ 7.9 GBd	sRJ/ RJ/ BUJ/ HF-PJ1[2]/ HF-PJ2[2]	For M8009A-062: 1 UI For M8009A-061 1 UI. For 99 to 105 GBd : 0.3 UI [1]
3.95 GBd to < 7.9 GBd	sRJ/ RJ/ BUJ/ HF-PJ1[2]/ HF-PJ2[2]	0.5 UI
< 3.95 GBd	sRJ/ RJ/ BUJ/ HF-PJ1[2]/ HF-PJ2[2]	0.25 UI

1. For ambient temperatures <28 °C.
2. The range is applicable when HF PJ modulation frequency is 500 MHz. For lower HF PJ modulation frequencies, see below.

The sum of RJ, sRJ, BUJ, HFPJ1 and HFPJ2 is calculated as follows: (A= jitter amplitude. f = jitter modulation frequency.

$$A_{BUJ} + A_{RJ} * 14 + A_{sRJHF} * 14 + A_{sRJLF} * 14 + \frac{A_{HFPJ1}}{\min\left(4, \frac{500\ MHz}{f_{HFPJ1}}\right)} + \frac{A_{HFPJ2}}{\min\left(4, \frac{500\ MHz}{f_{HFPJ2}}\right)} \leq \begin{cases} 0.25\ UI \text{ for } 2.0 \text{ to } 3.95\ GBd \\ 0.5\ UI \text{ for } 3.95 \text{ to } 7.9\ GBd \\ 1.0\ UI \text{ for } 7.9 \text{ to } 120\ GBd \end{cases}$$

The extended amplitude ranges for HFPJ1 and HFPJ2, shown in this formula, are supported.

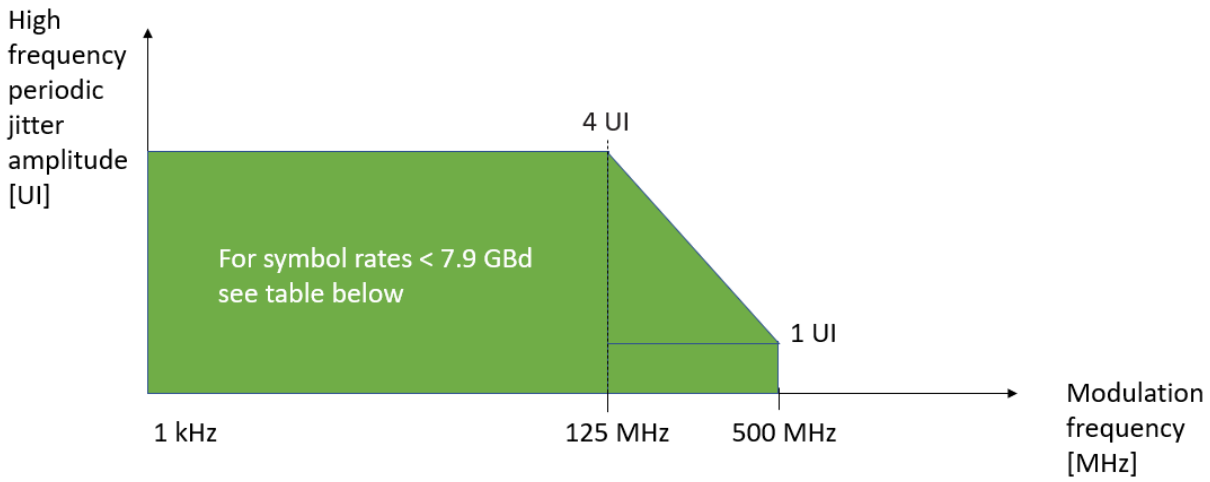

Figure 11. The high frequency jitter range depends on the selected symbol rate and the jitter modulation frequency. The graph shows the available range for one HF PJ source when all other HF jitter sources are off and for symbol rates above 7.9 GBd. For symbol rates below 7.9 GBd see table above.

Table 24. High-frequency periodic jitter modulation ranges (peak-peak)

Symbol rate	Max UI at modulation frequency between 1 kHz and 125 MHz	Max UI at modulation frequency 250 MHz	Max UI at modulation frequency 500 MHz
7.9 to 120.00 GBd	4.0 UI	2.0 UI	1.0 UI
3.95 to <7.9 GBd	2.0 UI	1.0 UI	0.5 UI
2.0 to <3.95 GBd	1.0 UI	0.5 UI	0.25 UI

Table 25. Specifications for high frequency periodic jitter, random jitter, bounded uncorrelated jitter (requires M8009A-0G3).

Parameter		
High frequency periodic jitter (HF PJ1, HF PJ2)	Range	See HF jitter above [1]
	Frequency	1 kHz to 500 MHz. Two tone possible
	Jitter amplitude accuracy	For M8009A-062: ±3 ps ±10% typical ±3 ps ±15% typical for symbol rates < 32.5 GBd and modulation frequencies > 100 MHz For M8009A-061: ±3 ps ±10% typical for symbol rates ≥ 32.5 GBd ±3 ps ±25% typical for symbol rates < 32.5 GBd
	Adjustable	For each channel independently
Random jitter (RJ)	Range	0 to 72 mUI rms max (1 UI p-p max) [1] See HF jitter above
	Jitter amplitude accuracy	For M8009A-062: ±300 fs rms ±10% typical for symbol rates ≥ 20.0 GBd ±300 fs rms ±20% typical for symbol rates < 20.0 GBd For M8009A-061: ±300 fs rms ±10% typical for symbol rates ≥ 32.5 GBd ±300 fs rms ±20% typical for symbol rates < 32.5 GBd
	Filters	High-pass: 10 MHz and "off", Low-pass: 100 MHz, 500 MHz, 1 GHz
	Adjustable	For each channel independently
	Crest factor	14 (peak-peak to rms ratio)
Spectrally distributed RJ according to PCIe 2 (sRJ)	Range	0 to 72 mUI rms max (1 UI p-p max) [1]
	Frequency	LF: 0.01 to 1.5 MHz, HF: 1.5 to 100 MHz
	Jitter amplitude accuracy	For M8009A-062: ±300 fs rms ±10% typical for symbol rates ≥ 20.0 GBd ±300 fs rms ±20% typical for symbol rates < 20.0 GBd For M8009A-061: ±300 fs rms ±10% typical for symbol rates ≥ 32.5 GBd ±300 fs rms ±20% typical for symbol rates < 32.5 GBd
	Adjustable	For each channel independently
Bounded uncorrelated jitter (BUJ)	Range	See HF jitter above [1]
	PRBS polynomials	2^n–1, n = 7, 8, 9, 10, 11, 15, 23, 31
	Filters	50/ 100/ 200 MHz low pass 3rd order 150/ 300 MHz low pass first order (20 dB/ decade)
	Jitter amplitude accuracy	For M8009A-062: ±5 ps ±10% typical for settings shown in table below For M8009A-061: ±5 ps ±10% typical for symbol rates ≥ 32.5 GBd ±5 ps ±20% typical for symbol rates < 32.5 GBd for settings shown in table below
	Rate for PRBS generator	625 Mb/s, 1.25 Gb/s, and 2.5 Gb/s
	Adjustable	For each channel independently
Clock/2 jitter	See M8042A data output	

1. Range of HF jitter applies to sum of RJ, HF-PJ1 and HF-PJ2, and BUJ. sRJ is mutually exclusive with RJ and BUJ. Valid if sRJ low pass filter is "on".

Table 26. BUJ accuracy applies for these conditions (requires M8009A-0G3).

Parameter [1]	Rate for PRBS generator	PRBS polynomial	Low pass filter
CEI 6G	1.25 Gb/s	PRBS 2^9–1	100 MHz
CEI 11G	2.5 Gb/s	PRBS 2^{11}–1	200 MHz
Gaussian	2.5 Gb/s	PRBS 2^{31}–1	100 MHz
CEI 25G	2.5 Gb/s	PRBS 2^{11}–1	200 MHz
CEI 56G	2.5 Gb/s	PRBS 2^{11}–1	200 MHz
IEEE 802.3ck	2.5 Gb/s	PRBS 2^7–1 PRBS 2^9–1	150 MHz
IEEE 802.3ck	2.5 Gb/s	PRBS 2^7–1 PRBS 2^9–1	300 MHz

1. Other settings are not calibrated and do not necessarily generate the desired jitter histograms for all data rates of the PRBS generator.

Table 27. Specifications for Spread Spectrum Clocking (SSC). SSC and segmented SSC are mutually exclusive. Requires M8009A-0G3 jitter modulation option.

Parameter		
SSC (spread spectrum clocking)	Symbol rate range for SSC	2 to 120.0 GBd
	Range [1] for center spread SSC	0 to 1% for symbol rates from 2 to 50.0 GBd For symbol rates from 50 to 120 GBd: max range is 50 GBd/ symbol rate * 1%. Example for 64 Gbd: max SSC deviation is 50/64 *1% = 0.78%
	Range [1] for asymmetric, down-spread, up-spread SSC: Upper deviation range Lower deviation range	0 to ± 1% for symbol rates up to 25 GBd For symbol rates from 25 GBd to 120 GBd: 25 GBd/ symbol rate * 1%. Example for 64 GBd: max SSC deviation = 25/64 *1% =0.39%
	Frequency	100 Hz to 200 kHz
	Modulation	Triangular and arbitrary modulation
	SSC amplitude accuracy	± 0.025% typical
	Outputs	Can be turned on/ off together for M8042A Data Out 1/2, Trg Out 1/2 and for M8009A Clk Out 16G and Channel Clk Out 1/2
Segmented SSC	Shape	Presets are available for: Universal Serial Bus (USB): USB4 10G, USB4 20G, USB4 40G, and DisplayPort (DP): DP RBR, DP HBR, DP HBR2, DP HBR3, DP UHBR10 User defined parameters: adjustable deviations from presets Custom: import of arbitrary waveforms for each segment
	Segments	Presets and user defined: 3 Custom: 1 to 4 Segment length: 32768 samples per segment
	SSC deviation range	See above range for asymmetric SSC
	SSC frequency	20 to 40 kHz
Residual SSC (rSSC)	Range	0 to 600 ps. Only for symbol rates ≤ 16 GBd.
	Modulation frequency	10 to 100 kHz
	Outputs	Can be turned on/off together for M8042A Data Out 1 and Trg Out 1 and for Data Out 2 and Trg Out2. Can be independently turned on/off for M8009A Clk Out 16G

1. Ranges are applicable when LF PJ and rSSC are turned off.

External Level Interference Sources

The Keysight M8053A and M8054A interference source and M8194A, M8195A and M8196A AWGs can be used as level interference source with sinusoidal and random modulation. The M8000 system software controls the interference parameters such as amplitude, bandwidth, crest factor. Keysight provides matched coupler pairs for injecting the RI or SI signal before and after the channel. See the table below for an overview.

For more details, please refer to the datasheet for M8053A, M8054A, M8195A, M8196A, M8194A.

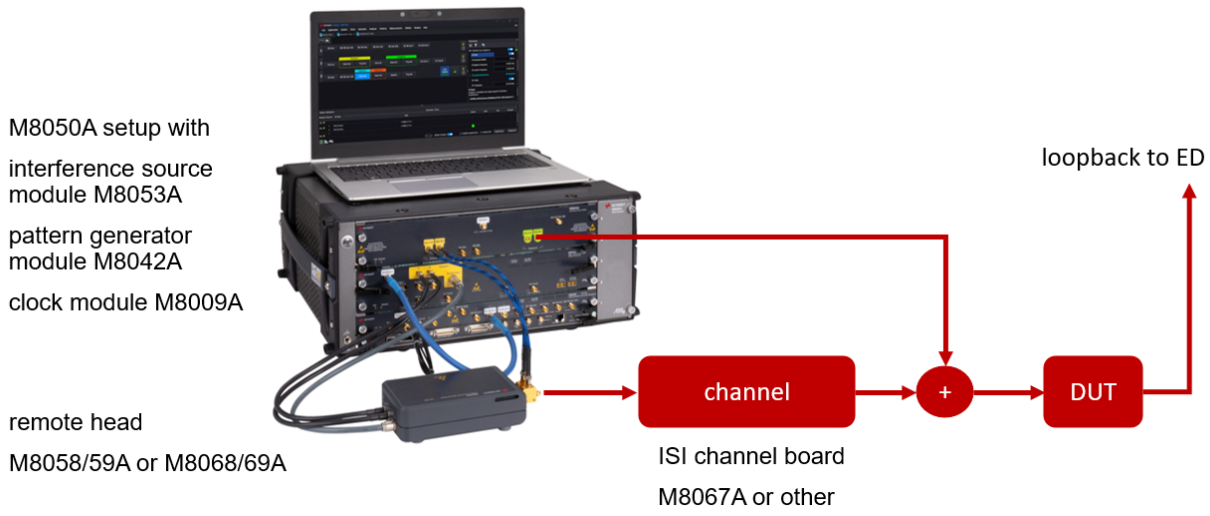

Figure 12. Keysight provides interference sources to be used in combination with M8050A to enable interference tolerance testing.

An overview of available interference sources from Keysight is shown in this table:

Model	Function	Description
M8053A Interference Source 64 GHz 	The Keysight M8053 interference source enables interference tolerance testing of highest-speed digital receivers supporting symbol rates above 64 GBd. Recommended for 1.6T receiver stress testing and future generations of PCIe.	• RI and SI up to 64 GHz • 2 differential channels • 2-slot AXIe module • Control from M8070B
M8054A Interference Source 32 GHz 	The Keysight M8054A interference source, can be used as level interference source with sinusoidal and random modulation (also called gaussian or white noise). Recommended for USB, PCIe, SATA, SAS, 400GbE receiver stress testing.	• RI and SI up to 32 GHz • 4 differential channels • 1-slot AXIe module • Control from M8070B
M8195A/ M8196A/ M8194A Arbitrary Waveform Generators	The Keysight M8195/6/4A AWGs are flexible sources with wide bandwidth suitable for multiple applications. They can also be used as level interference source with sinusoidal and random modulation.	• RI and SI up to 25/ 32/ 40 GHz • 4 differential channels • 1-slot AXIe module • Control from M8070B
81160A Pulse Function Arbitrary Noise Generator 500 MHz 	High precision pulse generators enhanced with versatile signal generation, modulation and distortion capabilities. Recommended for automotive Ethernet with symbol rates < 10 GBd.	• Noise up to 160 MHz • Sinewave up to 500 MHz • Stand-alone instrument

Emulation of ISI (Inter Symbol Interference)

Adjustable ISI (Intersymbol Interference) with M8070ISIB

The Adjustable ISI Software Package M8070ISIB simplifies receiver testing by offering the most flexible way for emulating channel loss for baud rates up to 120 Gbd. Up to a frequency range of symbol rate/ 2 a channel response can be emulated or de-embedded by the pattern generator by specifying a certain insertion loss at specific frequency points. This integrated channel emulation can be combined with actual physical ISI trace boards to result in a target test channel.

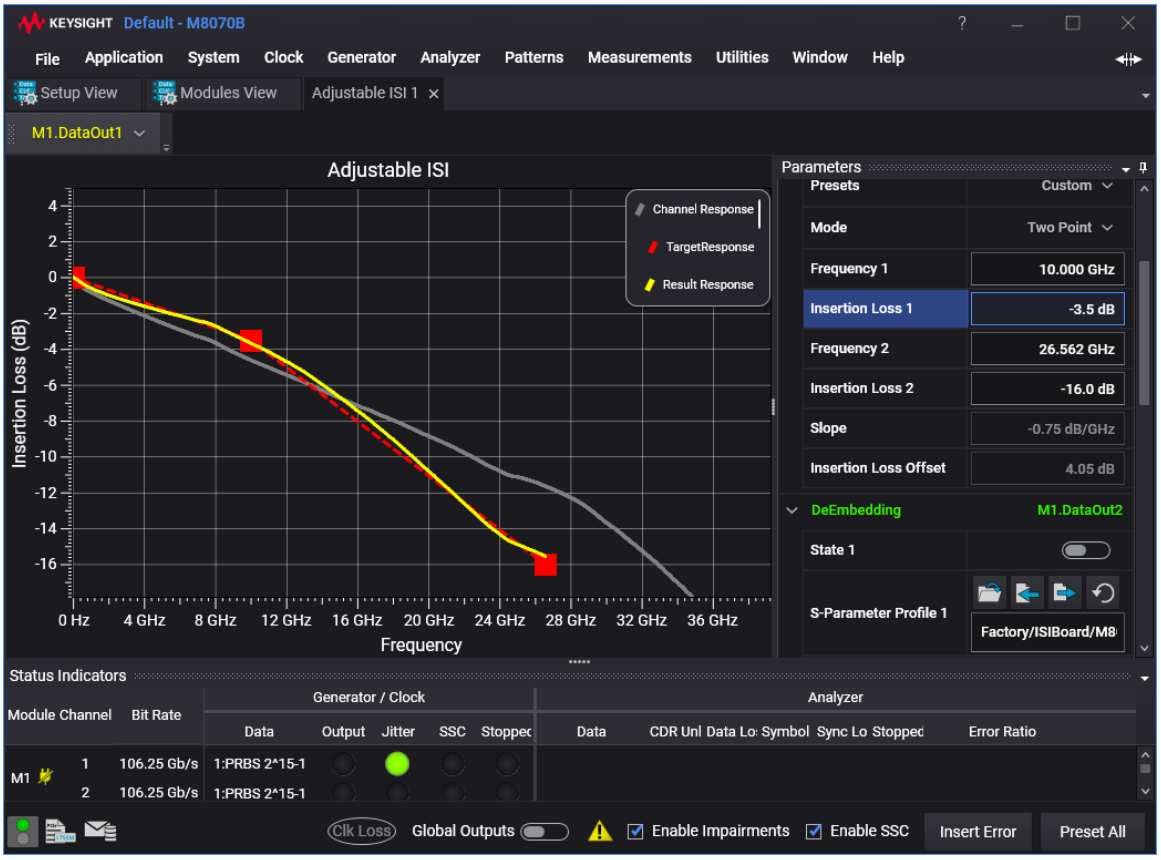

Figure 13. The adjustable ISI software package M8070ISI allows to emulate ISI internally with the M8042A pattern generator module. The example shows as channel response (gray) the insertion loss of an external ISI channel. You can add or remove insertion loss (red for target response) at 2 frequency points.

Table 28. Specifications for adjustable ISI M8070ISIB when used with M8042A

Parameters	M8070ISIB	
Supported symbol rates	2.000 to 120.0 GBd for M8042A-G12 2.000 to 64.8 GBd for M8042A-G64 2.000 to 32.4 GBd for M8042-G32 A channel response can be emulated or de-embedded up to a maximum frequency range of symbol rate / 2.	
ISI modes	One Point Two Point S-Parameter from s2p or s4p file with adjustable weight	
ISI insertion loss	Range[1] at symbol rate / 2 Resolution Accuracy	-20 dB to +10 dB 0.1 dB 0.1 dB typical
De-embedding	Up to two s2p or s4p files with adjustable weight	
Software download	For latest version see: https://www.keysight.com/us/en/support/M8070ISIB/adjustable-isi-channel-emulation-package-m8000-series-ber-test-solutions.html#drivers	
License types	Choose between node-locked, transportable, network, USB-dongle license types either perpetual or with limited duration. The network license is only recommended when using multiple M8050A setups within one company	
Pre-requisites	Requires M8042A pattern generator module with de-emphasis option (M8042A-0G4) M8070B software revision 9.5.350.6 or higher M8070ISIB software revision 1.0.100.6 or higher M8042A module driver 2.5.50.0 or higher	

1. The available loss range is referenced to the defined external ISI board or 0 dB if the external ISI board is set to NONE. It scales linearly from 0 Hz to symbol rate/ 2.

ISI Channel Boards

Keysight offers ISI channel boards M8067A that allow emulating a wide range of channel losses for symbol rates above 32 GBd. For symbol rates below 32 GBd we recommend using the M8049A ISI channel boards.

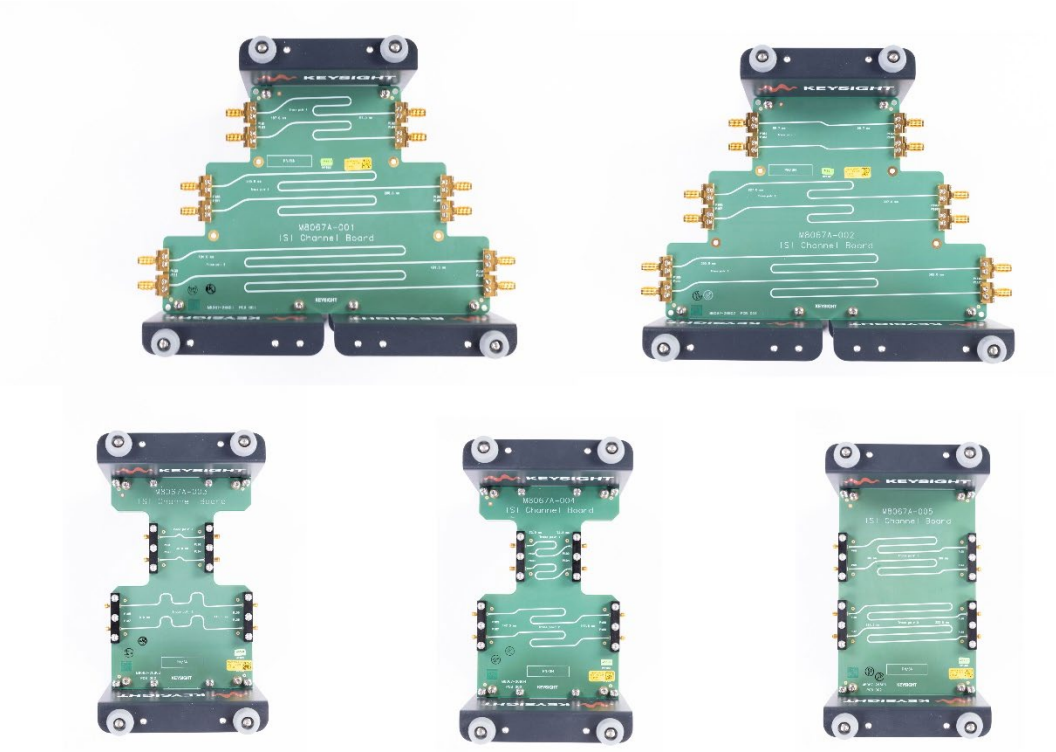

Figure 14. Keysight offers ISI channel boards M8067A-001, -002, -003, -004, and -005. The boards -001 and -002 offer 1.85 mm connectors and are suitable for emulating channel losses to characterize receivers that operate up to 64 GBd. For characterizing receivers that operate at symbol rates above 64 GBd and up to 120 GBd we recommend using the ISI channel boards M8067A-003, -004 or -005 with 1.0 mm connectors.

Please refer to the M8067A data sheet for more details.

Error Analysis

The M8043A and the M8046A error analysis modules can be used in combination with the M8042A pattern generator. For symbol rates above 64 GBd, realtime-oscilloscope based error analysis is supported. DUT's built-in error counter can be accessed for automated measurements such as jitter tolerance.

This table provides an overview of available error analysis choices for M8050A:

	M8043A	M8046A	UXR-based
Supported symbol rates @ PAM4	2.4 to 64 GBd	2.4 to 58 GBd	14-120GBd
Recommended for	400G, 800G, PCIe 128 GT/s	PCIe 64 GT/s and lower, USB	1.6T
Line codings	NRZ, PAM4	NRZ, PAM4, PAM3	NRZ, PAM4, PAM6, PAM8
Filtering of filler symbols	no	PCIe 2.5, 5, 8, 16, 32, 64 GT/s USB 5 and 10 Gb/s, dual lane	no
Interactive link training	no	PCIe 8, 16, 32, 64 GT/s USB 5 and 10 GT/s, dual lane	no

See the M8040A datasheet for M8046A specifications.

Specifications for error analyzer module M8043A and remote head M8052A

Figure 15. The error analyzer module M8043A provides one channel and occupies 2 slots in the AXIe chassis.

Figure 16. The analyzer remote head M8052A is required to operate the error analyzer module. The two cables on the back side of the remote head are used to connect with the M8043A error analyzer module.

The M8043A error analyzer module operates from 2.0 to 64.4 GBd. It requires the remote head M8052A. The built-in clock recovery works over the full symbol rate range and is included by default. Integrated equalization and de-embedding with FIR, FFE and CTLE is optional. For error analysis above 64.4 GBd we recommend using the UXR0802A/04A with control from M8070B. See below for more details.

Using the remote head input of the M8043A module directly without the M8052A is prohibited.

The following analyzer options are provided:

- Error analysis up to 32.4 GBd for NRZ and PAM4 (M8043A-A32). Includes internal clock recovery.
- Error analysis up to 64.4 GBd for NRZ and PAM4 (M8043A-A64). Includes internal clock recovery.
- Equalization, license (M8043A-0A3)

Keysight offers multiple software packages for advanced measurements and for error distribution analysis. Refer to the M8070ADVB and M8070EDAB sections below.

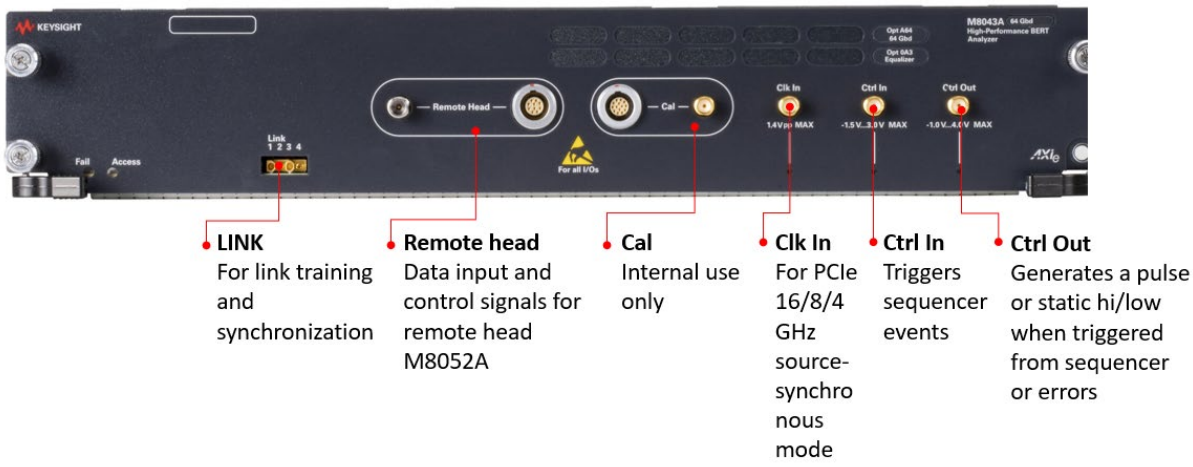

Figure 17. The M8043A analyzer module occupies two slots of the AXIe chassis. It requires to be operated with the remote head M8052A.

Data Input

All Data input specifications are valid at the input of the matched cable pair M8058A-801 (length 150 mm, 1.85 mm connectors) that is attached to the M8052A remote head.

Table 29. Data input characteristics of M8043A with M8052A. Only valid with M8052A remote head

Parameter	NRZ	PAM4
Symbol rate	M8043A-A32: 2.000 GBd to 32.400 GBd M8043A-A64: 2.000 GBd to 64.400 GBd	
Channels per module	1	
Line coding	NRZ, PAM4	
Input sensitivity, single-ended [1, 2]	For NRZ eye height: 26.5625 GBd: 15 mV typical 32.0 GBd: 15 mV typical 53.125 GBd: 18 mV typical 64.0 GBd: 20 mV typical All values for a BER of 10^{-12}	For PAM4 eye height: 26.5625 GBd: 16 mV per eye typical 32.0 GBd: 16 mV per eye typical 53.125 GBd: 22 mV per eye typical 64.0 GBd: 27 mV per eye typical All values for a BER of 10^{-12}
Input amplitude range	100 mVpp to 1.2 Vpp, differential 50 to 600 mVpp, single-ended	
Input voltage range	-1.0 V to +3.0 V	
Input resistance	Differential: 100 Ω ± 4 Ω typical Single ended: 50 Ω ± 2 Ω typical. Terminate unused input with 50 Ω.	
Input coupling	Selectable: AC coupled, or DC coupled	
Termination voltage range	-1.0 V to +3.0 V Termination must be within a window of DC common voltage ± 1.5V	
Input bandwidth, 3 dB	Symbol rate / 1.8 (nom.) Example: 64.4 GBd / 1.8 = 35.8 GHz (nom). The bandwidth is limited by a digital filter with Raised Cosine characteristic	
Timing resolution	1 mUI (nom.)	
Sampling point	Manual and automatic. Finds optimum voltage range, threshold and delay of the sampling point. Delay accuracy: ± 1 ps (nom.) One sampling edge per UI.	
Decision threshold range	-1.0 V to +3.0 V; full input voltage range	
Threshold resolution	1 mV (nom.)	
Equalization	Yes, requires M8043A option -0A3. See table below.	

Parameter	NRZ	PAM4
Phase margin [1, 2, 3]	26.5625 GBd: 0.83 UI typical 32.0 GBd: 0.83 UI typical 53.125 GBd: 0.80 UI typical 64.0 GBd: 0.63 UI typical All values for a BER of 10^{-12}	26.5625 GBd: 0.30 UI typical 32.0 GBd: 0.30 UI typical 53.125 GBd: 0.25 UI typical 64.0 GBd: 0.10 UI typical All values for a BER of 10^{-12}
Connectors	1.85 mm, female	

1. Measured with a PRBS 2^{15}-1
2. For single-ended operation: Terminate unused input externally with 50 Ω to GND
3. With M8042A pattern generator. Amplitude of input signal: 450 mVpp, single ended or 900 mVpp, differential.
4. Loss generated using a combination of M8067A ISI Channel Boards and Adjustable ISI Software Emulation M8070ISIB
5. Loss compensated using a combination of S-parameter based de-embedding and automatic coefficient optimization offered with M8043A-0A3
6. Differential operation

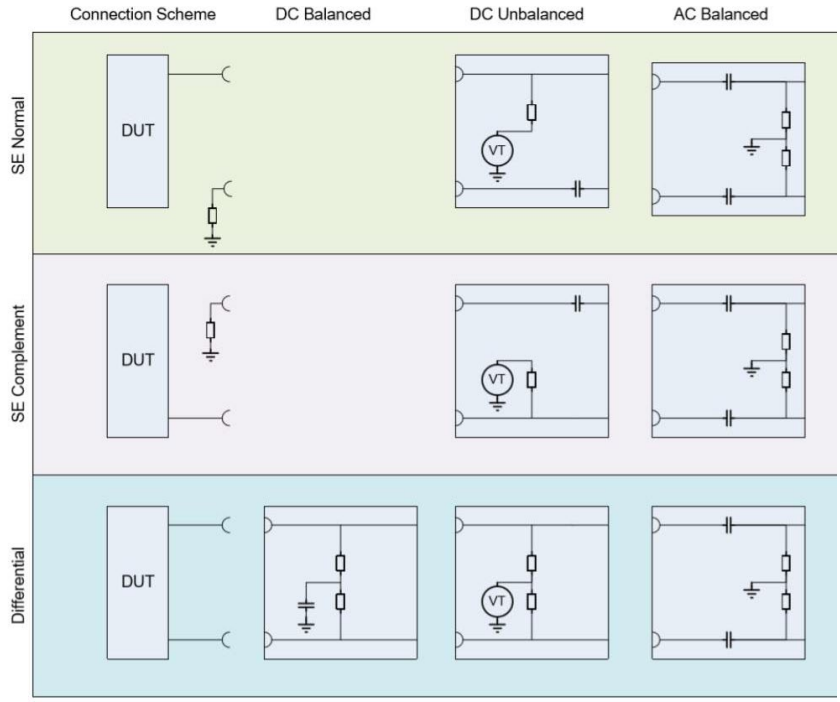

Figure 18. Connection and termination schemes for M8043A. To avoid floating offset: In “DC balanced, differential” mode, it is recommended to drive the input DC coupled.

Equalization and de-embedding for M8043A

The M8043A provides powerful equalization and de-embedding capabilities to compensate for losses in the backchannel.

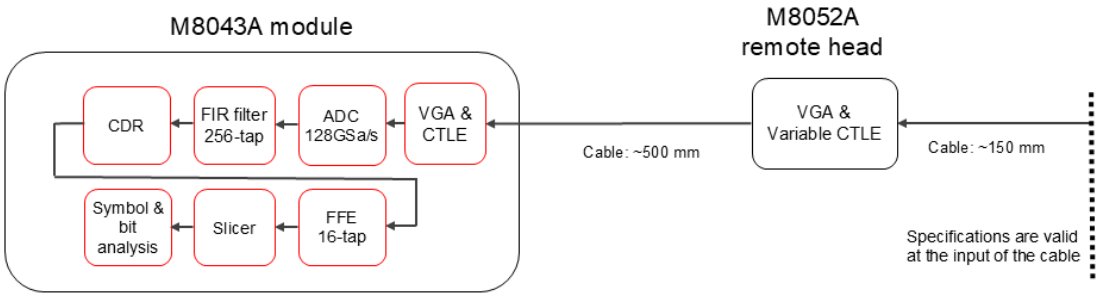

Figure 19. Block diagram of error analyzer module M8043A with M8052A remote head

Equalization

For equalization of the backchannel from the DUT to the M8043A, the M8043A uses a combination of a 256-tap FIR filter running at 128 GSa/s, and a 16-tap FFE (feed forward equalizer) running at the recovered symbol rate. To enable the equalization capability of the M8043A, Option -0A3 is required.

Table 30. Equalization characteristics for M8043A with M8052A (requires M8043A-0A3)

Parameter	
Equalizer modes	• Manual coefficient entry of the FFE. • Automatic coefficient optimization of the FFE. • Presets. Affects FIR filter
Manual FFE coefficient setting	16 filter coefficients numbered from 0 to 15. Coefficient 2 is the main-cursor and cannot be changed. The available value range is: • Coefficient 0: -0.25 to + 0.25 • Coefficient 1: -0.5 to + 0.5 • Coefficient 2: 1.0 • Coefficient 3: -0.5 to +0.5 • Coefficient 4: -0.25 to + 0.25 • Coefficient 5: -0.125 to +0.125 • Coefficient 6 to 15: -0.0625 to +0.0625 The sum of all 16 coefficients may not be 0
Automatic coefficient optimization	Requires an input signal with random-like pattern. It's an iterative procedure to minimize BER.
Pre-configured equalizer settings	The following pre-configured equalizer settings are available: PCIe 3.0 @ 8 GBd NRZ: - 12 dB to - 6 dB, Resolution: 0.1 dB PCIe 4.0 @16 GBd NRZ: - 12 dB to - 6 dB, Resolution: 0.1 dB PCIe 5.0 @ 32 GBd NRZ: - 15 dB to - 5 dB, Resolution: 0.1 dB PCIe 6.0 @ 32 GBd PAM4: - 15 dB to - 5 dB, Resolution: 0.1 dB PCIe 7.0 @ 64 GBd PAM4: - 15 dB to - 5 dB, Resolution: 0.1 dB (characteristic is based on PCIe7 version 0.3) CEI-112G @ 56 GBd PAM4: - 12 dB to - 2 dB, Resolution: 0.1 dB IEEE 802.3 200GAUI-4: - 9 dB to - 1 dB, Resolution: 0.1 dB
Loss compensation [1, 2, 3, 4, 5] for a BER of 10^{-12}	**NRZ** 26.5625 GBd: >30 dB (meas.) channel loss at 13.28 GHz 32.0 GBd: >30 dB (meas.) channel loss at 16.0 GHz 53.125 GBd: 30 dB (meas.) channel loss at 26.5625 GHz 64.0 GBd: 27 dB (meas.) channel loss at 32.0 GHz **PAM4** 26.5625 GBd:21 dB (meas.) channel loss at 13.28 GHz 32.0 GBd: 20 dB (meas.) channel loss at 16.0 GHz 53.125 GBd: 11 dB (meas.) channel loss at 26.5625 GHz 64.0 GBd: 10 dB (meas.) channel loss at 32.0 GHz

1. Measured with a PRBS 2^{15}-1. Differential operation.
2. With M8042A pattern generator. Amplitude of input signal: 450 mVpp, single ended or 900 mVpp, differential.
3. Loss generated using a combination of M8067A ISI Channel Boards and Adjustable ISI Software Emulation M8070ISIB
4. Loss compensated using a combination of S-parameter based de-embedding and automatic coefficient optimization of the FFE offered with M8043A-0A3
5. It's possible to combine equalization and de-embedding capabilities. Using the combination, loss compensation cannot get significantly improved beyond the specifications in table 32.

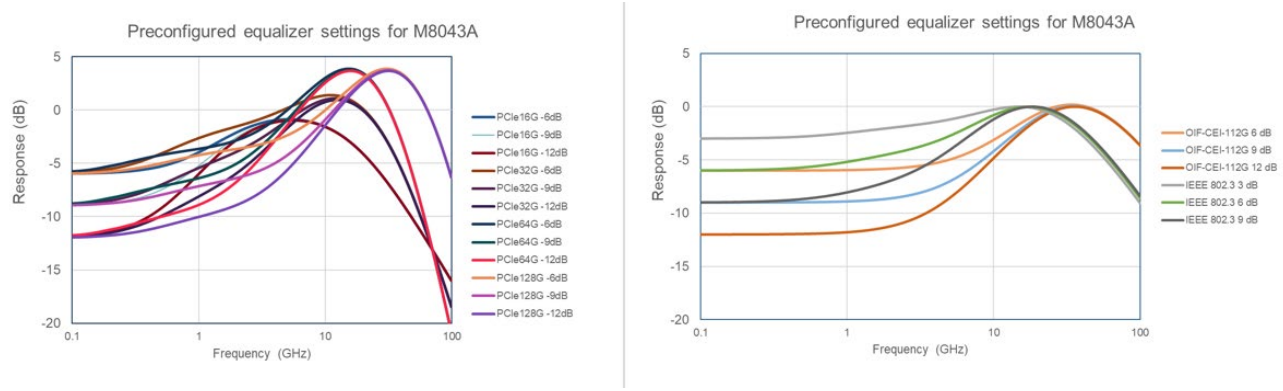

Figure 20. Preconfigured equalizer settings are available for the M8043A. The graph on the left shows typical PCIe responses for selected gains. Ethernet and OIF-CEI response characteristics are shown for selected gains in the graph on the right side. The gain can be adjusted in 0.1 dB steps over a wide range, as shown in the table above.

De-embedding

For de-embedding of the backchannel from the DUT to the M8043A, the M8043A uses a combination of CTLE (continuous time linear equalization) and a 256-tap FIR (finite impulse response) filter running at 128 GSa/s. The digital FIR filter offers very powerful and accurate de-embedding capability. The accuracy of the FIR filter based de-embedding is defined by filter length, and resolution. To enable de-embedding capability of the M8043A, Option -0A3 is required.

Two different modes for de-embedding can be selected:

1. Load S-parameter: S-parameters are loaded using S-parameter file import. The loss compensation capabilities of the M8043A are determined by the accuracy of the provided S-parameters.
2. Measure channel response: Frequency response of the backchannel is automatically measured by the M8043A.

Table 31. De-embedding capabilities for M8043A with M8052A loading S-parameters (requires M8043A-0A3)

Parameter	
De-embedding [1]	The following functionality can be enabled or disabled: • Entry of backchannel characteristics defined by loss in dB at a frequency in GHz. • S-Parameter profile 1, .s2p or .s4p with adjustable weight • S-Parameter profile 2, .s2p or .s4p with adjustable weight

1. De-embedding affects analog performance of data input such as e.g., sensitivity or phase margin.

Measure channel response: For de-embedding the M8043A measures frequency response of the backchannel. The measured frequency response is used to calculate the coefficients of the 256-tap FIR filter to compensate for channel loss and to minimize BER.

During the measurement of the channel response a predefined pattern must be applied to the M8043A. For correct operation of the algorithm and to achieve optimal results impairments such as e.g. SSC, PJ, ISI, shall be turned off.

Measurement of the channel response typically needs to be performed only once per test setup. The channel response measurement includes measurement of the input characteristic of the M8043A. To maintain optimum backchannel loss compensation, the input range of the M8043A shall not be changed while de-embedding using measured channel response is enabled.

After the channel response measurement of the backchannel is completed, any pattern including e.g. any PRBS as well as complex sequences can be analyzed with the M8043A. Also, impairments can be applied.

Table 32. De-embedding capabilities for M8043A with M8052A in 'Measure channel response' mode.

Parameter	
Measure channel response mode	• Automatic coefficient optimization of the FIR filter and CTLE. • Enable or disable
Predefined pattern	Requires an input signal with a predefined pattern with the following characteristics: - Minimum length: 1023 Symbols - Maximum length: for symbol rate < 16 GBd: 8192 symbols for symbol rate 16 GBd to 64.4 GBd: 32 ksymbols - NRZ or PAM4 - Transition density: ~0.5 - Max. run length of zeroes and ones: 31
Execution time for 'Measure channel response'	26 GBd to 32 GBd: PRBS 2^{10}-1: 95 s (meas.) 26 GBd to 32 GBd: PRBS 2^{15}-1: 320 s (meas.) 53 GBd to 64 GBd: PRBS 2^{10}-1: 90 s (meas.) 53 GBd to 64 GBd: PRBS 2^{15}-1: 200 s (meas.) Values apply for PAM4 line coding

Parameter	NRZ [1, 2, 3, 4, 5]	PAM4 [1, 2, 3, 4, 5]
Loss compensation for a BER of 10^{-12}	26.5625 GBd: >36 dB (meas.) channel loss at 13.28 GHz 32.0 GBd: >36 dB (meas.) channel loss at 16.0 GHz 53.125 GBd: 34 dB (meas.) channel loss at 26.5625 GHz 64.0 GBd: 30 dB (meas.) channel loss at 32.0 GHz	26.5625 GBd: 26 dB (meas.) channel loss at 13.28 GHz 32.0 GBd: 26 dB (meas.) channel loss at 16.0 GHz 53.125 GBd: 24 dB (meas.) channel loss at 26.5625 GHz 64.0 GBd: 24 dB (meas.) channel loss at 32.0 GHz
Loss compensation for a BER of 10^{-9}	26.5625 GBd: >36 dB (meas.) channel loss at 13.28 GHz 32.0 GBd: >36 dB (meas.) channel loss at 16.0 GHz 53.125 GBd: >36 dB (meas.) channel loss at 26.5625 GHz 64.0 GBd: 35 dB (meas.) channel loss at 32.0 GHz	26.5625 GBd: 27 dB (meas.) channel loss at 13.28 GHz 32.0 GBd: 27 dB (meas.) channel loss at 16.0 GHz 53.125 GBd: 26 dB (meas.) channel loss at 26.5625 GHz 64.0 GBd: 26 dB (meas.) channel loss at 32.0 GHz
Loss compensation for a BER of 10^{-6}	26.5625 GBd: >36 dB (meas.) channel loss at 13.28 GHz 32.0 GBd: >36 dB (meas.) channel loss at 16.0 GHz 53.125 GBd: >36 dB (meas.) channel loss at 26.5625 GHz 64.0 GBd: 36 dB (meas.) channel loss at 32.0 GHz	26.5625 GBd: 34 dB (meas.) channel loss at 13.28 GHz 32.0 GBd: 34 dB (meas.) channel loss at 16.0 GHz 53.125 GBd: 29 dB (meas.) channel loss at 26.5625 GHz 64.0 GBd: 29 dB (meas.) channel loss at 32.0 GHz

1. Measured with a PRBS 2^{15}-1. Differential operation.
2. With M8042A pattern generator. Amplitude of input signal: 450 mVpp, single ended or 900 mVpp, differential.
3. Loss generated using a combination of M8067A ISI Channel Boards and Adjustable ISI Software Emulation M8070ISIB.
4. Loss compensated using 'Measure Channel response' mode offered with M8043A-0A3.
5. It's possible to combine equalization and de-embedding capabilities. Using the combination, loss compensation cannot be significantly improved beyond the specifications in this table.

CDR and source-synchronous mode

CDR mode of operation: The M8043A has an integrated Clock Data Recovery (CDR) which is always enabled. It operates for symbol rates from 2.0 to 64.4 GBd.

Source-synchronous mode of operation: The M8043A offers source-synchronous operation for symbol rates of 8, 16, 32, and 64 GBd. By applying the same SSC profile at the data input as on clock input of M8043A, data with SSC profiles having high deviation can be analyzed. In source-synchronous mode the CDR is enabled to automatically compensate for residual SSC or skew between clock input and data input.

CDR characteristics

Table 32. Clock data recovery characteristics for M8043A with M8052A

Parameter	
Clock recovery supported symbol rate range	M8043A-A32: 2.0 to 32.4 GBd for NRZ and PAM4 M8043A-A64: 2.0 to 64.4 GBd for NRZ and PAM4
Loop bandwidth	1.1 MHz (nom.)
Transition density	25% to 100% (nom.)
Capture range	For symbol rates 2.0 to 7.9 GBd: ± 500 ppm typical For symbol rates 7.9 to 15.8 GBd: ± 300 ppm typical For symbol rates 15.8 to 31.6 GBd: ± 150 ppm typical For symbol rates 31.6 to 64.4 GBd: ± 75 ppm typical
SSC tracking range[1]	For symbol rate: 16 GBd: Deviation ± 1500 ppm measured For symbol rate: 32 GBd: Deviation ± 750 ppm measured For symbol rate: 64 GBd: Deviation ± 250 ppm measured SSC tracking range in source-synchronous mode is shown in table 34
CDR freeze	Provided

1. SSC type: Center spread; SSC frequency: 33 kHz. All values for a BER 10^{-12}

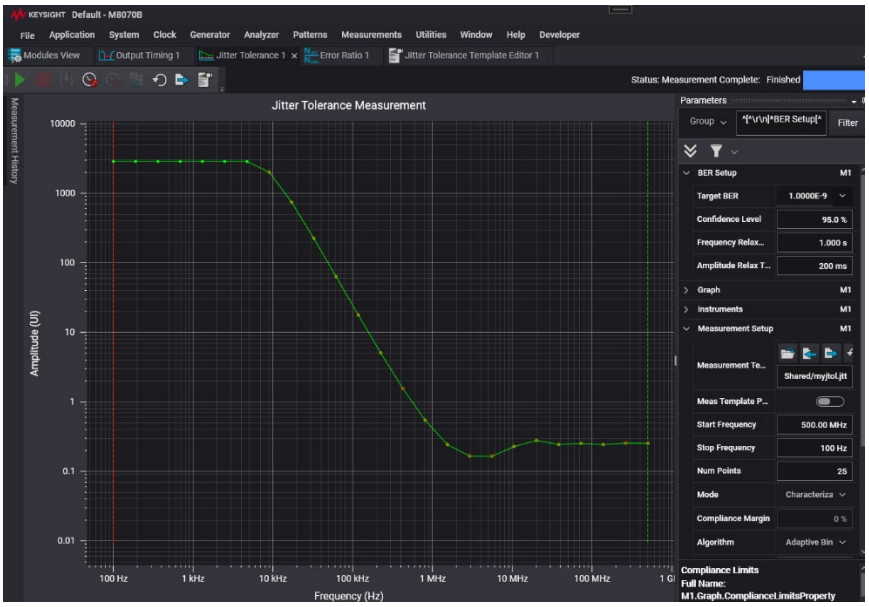

Figure 21. The M8042A can be used for jitter tolerance measurements. The example shows a jitter tolerance measurement at 53.125 GBd PAM4 PRBS pattern in direct loopback from the M8042A pattern generator when all other impairments are turned off. This measurement uses CDR mode. Source-synchronous mode is not enabled.

Source-synchronous mode

This clock input is designed for source-synchronous operation of the M8043A. Source-synchronous operation allows the M8043A to analyze data with SSC. The M8043A's CDR is also enabled in source-synchronous operation to compensate for skew and residual jitter between clock and data. For optimal SSC tracking of the M8043A the residual jitter shall be minimized by adjusting the delay between clock and data to ensure the phase of SSC profiles are the same on Data Input and Clock Input applied to the M8043A.

Sources for Clock Input and Data Input of the M8043A can be generated by e.g. the DUT. Source-synchronous operation can also be achieved by connecting Clock Input of the M8043A to the Clock Output 32G of the M8009A. In this configuration Data Output generated by the M8042A pattern generator can be connected to the DUT. The DUT sends the data back to the M8043A Error Detector for analysis.

Clock Input operation requires M8043A with serial number above MY64A01000.

Table 33. Clock Input characteristics for M8043A

Parameter	
Input frequency	Selectable: 4 GHz, 8 GHz or 16 GHz
Frequency accuracy	- 3000 ppm to + 500 ppm (typ.)
Input level	502 mV_{pp} (-2 dBm) to 1.4 V_{pp} (+7 dBm) (typ.)
Input impedance	50 Ω (nom.), AC coupled
Connector	SMA, female

Table 34. Source-synchronous mode of operation of M8043A

Parameter	
Symbol rates	8 GBd, 16 GBd, 32 GBd or 64 GBd for NRZ and PAM4
SSC tracking range [1]	Deviation: - 6000 ppm to + 1000 ppm (typ.)

1. SSC frequency: 33 kHz. All values for a BER 10^{-12}. SSC phase delay between Clock In and Data in less than ± 10ns

Control Input (Ctrl In)

Functionality can be selected as: sequence trigger, pattern capture event.

Table 35. Control input characteristics for M8043A

Parameter	
Input voltage range	–1 V to +3 V
Termination voltage range	–1 V to +3 V
Termination voltage accuracy	± 25 mV ± 1 %
Threshold	Range: –1 V to +3 V Accuracy: ± 50 mV typical
Response time	In pattern capture mode: 64 GBd: ~ 30 ns (measured) up to < 0.7 µs (measured) at 2 GBd

	In pattern sequencer control mode: 64 GBd: ~ 2.5 µs (measured) 2 Gbd: ~ 2.5 µs to 3.2 µs (measured)
Input impedance	50 Ω (nom.)
Connector	SMA, female

Control Output (Ctrl Out)

Outputs a pulse in case of an error. Generates a pulse or static high/low if used from sequencer.

Table 36. Control output characteristics

Parameter	
Amplitude	Range: 0.1 to 2 V Accuracy: ± 10 mV ± 2 % typical
Output voltage range	–0.5 to 1.75 V
Delay from data input	64 Gb/s NRZ: ~ 1 µs ± 30 ns (measured) 2 Gb/s NRZ: ~ 4 µs ± 0.7 µs (measured) For PAM4 line coding values are slightly smaller
Output impedance	50 Ω (nom.)
Connector	SMA, female

Communication Link (LINK)

The communication link is for future use.

Calibration Output (Cal Out)

The calibration output is used for factory calibration at Keysight facilities. It is not intended for use by customers.

Measurements

Table 37. Measurement capabilities for M8043A and M8046A when used with M8042A. For measurements with UXR-based error analysis see the table below.

Measurement		M8070B	M8070ADVB	M8070EDAB
BER, SER	Accumulation and instantaneous	Yes		
Jitter tolerance		No	Yes	
Counters	Compared bits, errored bits Compared 0 bits, errored 0 bits Compared 1 bits, errored 1 bits Compared symbols, errored symbols Compared symbols 0, 1, 2, 3 Errored symbols 0, 1, 2, 3	Yes		

BER Scan with RJ, DJ separation		No	Yes [1]	
Output level and Q-factor		No	M8043A: yes. NRZ M8046A: no	
Sampling point view		Yes		
BER versus parameter automated sweep		No	Yes	
BER Based Deemphasis	Optimize PG de-emphasis to minimize BER (via error analyzer or DCI)	No	Yes	
Error distribution analysis	See M8070EDAB details below.	No	No	M8043A: yes M8046A: yes
Pattern capture		Yes		
Masking	Expected bits can be masked during error counting. >Bitwise and block-wise masking is possible.	Yes		
Eye diagram, histogram based		No	M8043A: yes. PAM4 and NRZ M8046A: no	
Eye diagram, BER based		No	M8043A: yes. NRZ only M8046A:no	

1. The measurement is available in the user interface, but just for debugging/troubleshooting purposes. The accuracy of jitter separation results is unspecified in the case of NRZ and invalid in case of PAM4 signals.

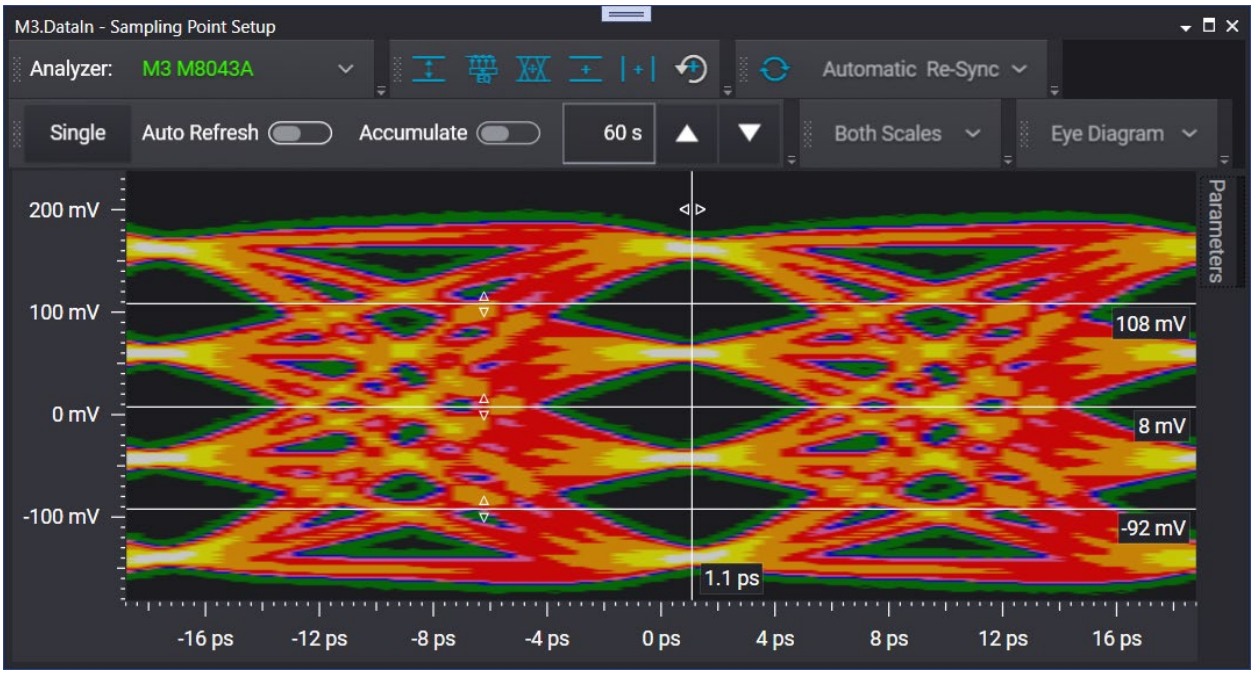

Figure 22. You can monitor the eye diagram based on a histogram with M8043A and the M8070ADVB measurement package. The example shows a 53.125 GBd PAM4 signal from a direct loopback to the pattern generator M8042A.

Error Analysis of Signals above 64 GBd based on Infiniium UXR Series Oscilloscopes

For analyzing errors of PAM4 up to 64 GBd the M8043A error analyzer module can be used.
For analyzing errors up to 58 GBd and support of interactive link training, the M8046A error analyzer module can be used. See the M8040A datasheet for details.

For symbol rates above 64 GBd, the Keysight M8000 system software supports the use of Keysight real-time oscilloscopes for capturing the signal and decoding it into a pattern stream. The M8000 system software uploads the acquired pattern and handles the synchronization and comparison with the expected pattern, even for long PRBS polynomials such as PRBS31Q. This method allows measuring target BERs of up to 10^{-6} or 10^{-7} for symbol rates up to 120 GBd within measurement times of about 1 minute. The real-time oscilloscope provides uniquely adjustable equalization and an integrated clock recovery supporting symbol rates up to 120 GBd.

See table below for more details.

Figure 23. The M8070ADVB controls the UXR and uploads the decoded pattern streams for synchronization and comparison with expected patterns.

Table 38. Conditions for error analysis with M8070ADVB using a real-time oscilloscope for symbol acquisition.

Parameter	Description
Supported real-time oscilloscope models	Keysight UXR series, all models from 59 to 110 GHz (2 or 4 channels)
Symbol rates	Maximum symbol rate is limited by UXR model: 14 GBd to 60 GBd for UXR0402/4A or B 14 GBd to 75 GBd for UXR0502/4A or B 14 GBd to 96 GBd for UXR0592/4A or B, 14 GBd to 105 GBd for UXR0702/4A or B, 14 GBd to 120 GBd for UXR0802/4A or B 14 GBd to 120 GBd for UXR1002/4A or B 14 GBd to 120 GBd for UXR1102/4A or B
Hardware acceleration	Hardware acceleration is active for 256 GSa/s UXR models when parameters are set in M8070ADVB to meet all of the following conditions: • Symbol rate: 51.2 GBd to 120 GBd • CDR type: 2nd order PLL • CDR loop bandwidth: Symbol rate / 2655 to Symbol rate / 500 Measurements are: • 1.8 times faster (meas.) for JTOL measurements • 2.5 to 3.5 times faster (meas.) for BER measurements When hardware acceleration is active. Display shall be turned OFF to achieve fastest measurement times. Factor of acceleration depends on parameter settings of the UXR such as e.g., line coding, baud rate, bits per acquisition and is provided as an estimation.
Target BER	Hardware acceleration active: ~10^{-7} Hardware acceleration inactive: ~10^{-6}
Coding	NRZ, PAM4, PAM6, PAM8
Pattern capture	Yes
Masking	Expected bits can be masked (ignored) during error counting. Bitwise and block-wise masking is possible.
Expected patterns	User definable: PRBS 2^n-1 with n = 7, 9, 10, 11, 13, 15, 23, 31, 33, 35, 39, 41, 45, 47, 49, 51 Memory patterns with max. pattern length of 256 kbit
Measurements	• Jitter tolerance, BER and SER • Error distribution analysis (restrictions with respect to memory depth of UXR to be able to capture maximum frame length may apply) • Automated parameter sweep versus BER
Measurement time	Depends on: • Expected pattern type • Expected pattern length (in case of memory patterns) • Symbol rate • Equalizer usage and parameters • Acquisition depth in UI • Target BER and confidence level

Parameter	Description
BER and symbol counters	BER counters: • Compared bits • Errored bits • Compared 0 bits, compared 1 bits • Errored 0 bits, errored 1 bits Symbol counters: • Compared symbols • Errored symbols For each symbol level: • Compared symbols Errored symbols
Error distribution statistics	Yes, for details see table 41. Requires M8070EDAB
Parameters	Acquisition Number of bits per acquisition. (Note: The maximum number of bits per acquisition is limited by the oscilloscope's acquisition memory depth, symbol rate and clock recovery setting.) • Global acquisition bandwidth limit • Channel bandwidth limit and filter type • Pattern capture up to 100 Mbit Horizontal reference clock: internal, external 10 MHz and 100 MHz Clock: Follow Sys Clock, symbol rate Line Coding: • Coding (NRZ, PAM4, PAM6, PAM8) • Symbol mapping (uncoded, Gray, custom) • Custom symbol mapping Comparator: • Compare mode (single ended / differential) • Polarity (non-inverted / inverted) • Auto-set thresholds • User-defined thresholds Equalizer • FFE- Number of taps and pre-taps • FFE - Auto-set coefficients • CTLE - DC gain • CTLE - Frequency pole #1, Frequency pole #2, • CTLE - Frequency zero #1 • DFE- Taps • DFE-Auto-set coefficients Clock Recovery (2nd Order CR) • Loop bandwidth • Symbol rate divider • Damping factor Sample delay (PAM4 only) Auto alignment • Covers thresholds, sample delay and equalizer coefficients Automatically set scope parameters: • Thresholds • FFE coefficients (cannot be changed by user) • Sample delay position (in case of NRZ)

Parameter	Description
Software pre-requisites	UXR: Infiniium version 11.40.00202 or higher and M8070B: M8000 system software. See table 41 for minimum required software revision M8070ADVB advanced measurement package software. See table 41 for minimum required software revision.
Measurement packages	Following licenses are required on the oscilloscope in addition: D9010PAMA Pulse Amplitude Modulation PAM-N analysis software D9020ASIA Advanced signal integrity software (EQ, InfiniSim, Advanced crosstalk)
Connection to UXR	LAN recommended

User Interface and Remote Control

The M8070B system software for M8000 series of BER measurement solutions is required to control the M8050A BERT. The user interface supports controlling combinations of M8050A and with other hardware of the M8000 Series.

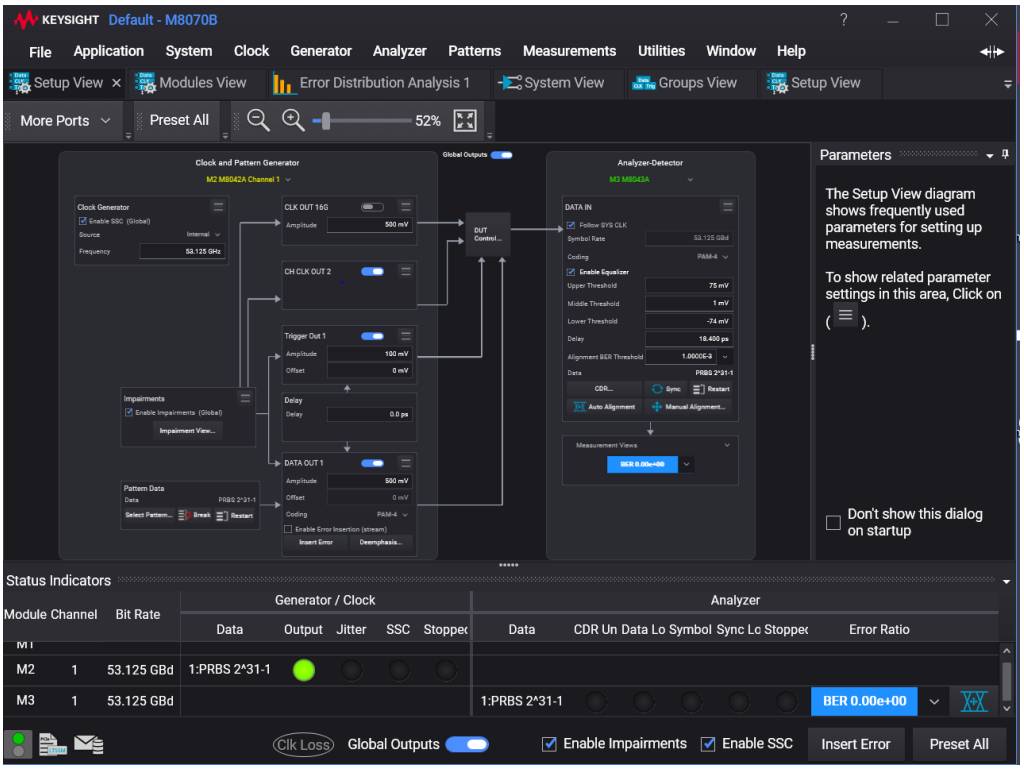

Figure 24. The M8070B system software is required to control the M8050A high-performance BERT. The user interface provides control of all parameters. It provides a graphical user interface and remote control via SCPI. Shown is the setup view with the M8009A clock module, the M8042A pattern generator module, and the M8043A error analyzer module on the right side.

M8070B system software for the M8000 Series of BER measurement solutions

Table 39. User interface and remote-control interface M8070B

Parameter	
Programming language	SCPI
Remote control interface	LAN
Save/Recall	Yes
Software update	Under the help menu the M8070B can show if there are newer SW revisions of M8070B, M8070ADVB, M8070EDAB, M8070ISIB, and M8042A, M8009A, M8043A module driver packages available for download from K.com.
SCPI recorder	Allows recording of the SCPI commands that correspond to the interactive control in the GUI. This includes: Parameter changes Sequence and pattern configuration Measurement creation, configuration and execution Group configuration Save and recall of settings The recorded SCPI commands can be copied to the clipboard or saved to a file for later playback.
Software download	For latest version of M8050A module drivers see: https://www.keysight.com/us/en/support/M8050A/120-gbd-high-performance-bert.html#drivers For latest version of M8070B system software see: https://www.keysight.com/us/en/lib/software-detail/computer-software/m8070b-system-software-3021035.html
Offline version	Yes. Can be used without M8000 hardware connected.
License types	Not licensed. Free baseline software

M8070ADVB advanced measurement package

Table 40. Features of the advanced measurement software package M8070ADVB

Advanced measurements	M8070ADVB
Measurements	See table measurements
Export of measurement results	Jitter tolerance results as *.csv file
Controlling other instruments via M8070B	Real-time oscilloscopes, e.g. DASZ634A, UXR0804A/B DCA oscilloscopes, e.g. N1046A, N1060A, N1094A/B, 86108B,
Scripting interface	The built-in scripting engine is based on IronPython. It enables the control of the device under test as well as another test equipment. Function hooks are available to tailor your measurements, such as read-out of built-in error counters or initializing the device
DUT control interface	Enables access to built-in error counters and status registers of a device under test (BIST) for use with automated measurements like accumulated BER and jitter tolerance. Can also be used to customize the measurements to DUT specific needs. IronPython scripting and .net libraries are supported to interface with the DUT
Auto-optimizing de-emphasis taps	DE taps are calculated for best eye height. Output levels are adjusted to the measured amplitude on the reference plane. If necessary, external attenuators can be considered to adjust higher voltages. Can be combined with embedding/de-embedding of s-parameter files.
Software download	For latest version see: https://www.keysight.com/us/en/support/M8070ADVB/advanced-measurement-package-m8000-series-bert-test-solutions.html#drivers
License types	You can choose between node-locked, transportable, perpetual license, network, USB-dongle license types with 6/12/24 month duration. The network license is only recommended when using multiple M8050A setups within one company

M8070EDAB error distribution analysis package

Table 41. Features of the error distribution analysis package M8070EDAB

Error distribution analysis	M8070EDAB
Measurements	• Frame loss ratio estimation (real-time update with M8046A) • Error map • Symbol-errors per frame distribution (real-time with M8046A) • Consecutive error distance distribution • Error burst count, capture and analysis (M8046A only)
Supported hardware	M8043A and M8046A UXR real-time oscilloscope (in combination with M8070ADVB plugin)
Software download	For latest version see: https://www.keysight.com/us/en/support/M8070EDAB/error-distribution-analysis-m8000-series-bert-test-solutions.html#drivers
License types	You can choose between node-locked, transportable, perpetual license, network, USB-dongle license types with 6/12/24 month duration. The network license is only recommended when using multiple M8050A setups within one company

Table 42. System requirements for M8050A and M8070B System Software

Parameter	
M9537A 1-slot AXIe embedded controller requirements	Choose M8050A-BU3 or -BU5 for a pre-installed embedded controller M9537A including pre-installation of M8070B software and module licenses. M8050A-BU3 and -BU5 are pre-configured with Windows 10. Otherwise: M9537A 1-slot AXIe embedded controller, choose options for Windows 10, 8 or 16 GB RAM, SSD.
External PC	Connection to AXIe chassis: USB 2.0 (Mini-B) recommended or PCIe 2.0/8x (only for highest data throughput and desktop PC) or Thunderbolt (only for M9506A). Hot plugging supported. Memory: Minimum of 8 GB RAM recommended
Operating system	Windows 10, Windows 11
Display resolution	Minimum requirement 1024 x 768
Software pre-requisites	Keysight IO Libraries Suite 2024 Update 2 Build 21.1.17 or newer M9505A AXIe 5-slot chassis firmware: Version 2.1.6 or newer M9502A AXIe 2-slot chassis firmware: Version 2.1.6 or newer M8070B: Version 11.6 or newer M8070ADVB: Version 1.13.170.12 or newer M8070EDAB: Version 1.12.150.2 or newer M8070ISIB: Version 1.4.150.2 or newer M8042A module driver: Version 5.0 or newer M8009A module driver: Version 5.0 or newer M8043A module driver: Version 4.5 or newer

General Characteristics and Physical Dimensions

General characteristics for M8050A

Table 43. General characteristics for M8042A, M8009A modules and M8058A, M8059A remote heads.

Parameter	
Operating temperature	For configurations using M8009A-062: 5 °C to 40 °C For configurations using M8009A-061: 5 °C to 35 °C
Storage temperature	–40 to +70 °C
Operating humidity	15 to 95% relative humidity at 40 °C (non-condensing)
Storage humidity	24 to 90% relative humidity at 65 °C (non-condensing)
Operating altitude	Up to 2000 m
Physical dimensions	See tables below
Weight net	See tables below
Weight shipping	See tables below
Power consumption	See tables below
Interface to controlling PC	PCIe or USB or Thunderbolt
Recommended recalibration period	2 years
Warm-up time	30 minutes
Cooling requirements	Slot air flow direction is from right to left. When operating the M8050A choose a location that provides at least 80 mm of clearance at each side. See also start-up guide for M9505A chassis.
EMC tested acc. to	IEC 61326-1
Safety tested acc. to	IEC61010-1, ANSI/UL61010, CSA22.2 No. 61010-1
Quality management	ISO 9001, 14001

Physical dimensions and power for M8042A

Table 44. Physical dimensions and power requirements of the M8042A pattern generator module

	M8042A-0G1 (1 channel version)	M8042A-0G2 (2 channel version)
Form factor	2-slot AXIe module	3-slot AXIe module
Physical dimensions (W x H x D)	351 mm x 61 mm x 315 mm	351 mm x 92 mm x 315 mm
Power requirements	300 W (nom.)	600 W (nom.)
Weight net	6.1 kg	8.5 kg
Weight shipping	9.6 kg	12.0 kg

Physical dimensions for M8058A and M8059A

Table 45. Physical dimensions and power requirements of the M8058A and M8059A generator remote heads

Parameter	
Physical dimensions (W x H x D)	157 mm x 90 mm x 44 mm (remote head without cables)
Physical dimensions (W x H x D)	~810 mm x 90 mm x 44 mm (remote head with cables) Length of cable connection between M8058A/59A and M8042A module: ~500 mm Length of M8058A/M8059A: 157 mm Length of cable between M8058A/M8059A and DUT: ~150 mm
Weight net	1.0 kg
Weight shipping	Shipment of one Remote Head 3.7 kg Shipment of two Remote Heads 4.7 kg

M8042A ~500 mm cable M8058A ~150 mm, 1.85 mm cable

M8042A ~500 mm cable M8059A ~150 mm, 1.0 mm cable

Physical dimensions for M8068A and M8069A

Table 46. Physical dimensions and power requirements of the M8068A and M8069A generator remote heads

Parameter	
Physical dimensions (W x H x D)	157 mm x 101 mm x 59 mm (remote head without cables)
Physical dimensions (W x H x D)	~810 mm x 101 mm x 59 mm (remote head with cables) Length of cable connection between M8068A/69A and M8042A module: ~500 mm Length of M8068A/M8069A: 157 mm Length of cable between M8068A/M8069A and DUT: ~150 mm
Weight net	1.3 kg
Weight shipping	Shipment of one Remote Head 4.0 kg Shipment of two Remote Heads 5.0 kg

M8042A ~500 mm cable M8068A ~150 mm, 1.85 mm cable

M8042A ~500 mm cable M8069A ~150 mm, 1.0 mm cable

Physical dimensions and power requirements for M8009A

Table 47. Physical dimensions and power requirements of the M8009A clock module

Parameter	
Form factor	1-slot AXIe module
Physical dimensions (W x H x D)	351 mm x 30 mm x 315 mm
Power requirements	200 W (nom.)
Weight net	3.9 kg (meas.)
Weight shipping	7.5 kg (meas.)

Physical dimensions and power requirements for M8043A

Table 48. Physical dimensions and power requirements of the M8043A analyzer module

Parameter	
Form factor	2-slot AXIe module
Physical dimensions (W x H x D)	351 mm x 60 mm x 305 mm
Power requirements	320 W (nom.), includes power for M8052A remote head
Weight net	4.8 kg (meas.)
Weight shipping	9.8 kg (meas.)

Physical dimensions for M8052A

Table 49. Physical dimensions and power requirements of the M8052A analyzer remote head

Parameter	
Physical dimensions (W x H x D)	160 mm x 85 mm x 45 mm (remote head without cables)
Physical dimensions (W x H x D)	~810 mm x 85 mm x 45 mm (remote head with cables) Length of cable between M8043A and M8052A module: ~500 mm Length of M8052A: 160 mm Length of cable between M8052A and DUT: ~150 mm
Weight net	1.0 kg, including cables
Weight shipping	3.5 kg

M8043A ~500 mm, 1.85 mm cable M8052A ~150 mm, 1.85mm cable

Physical dimensions for M8050A-BU2, -BU3, -BU4, and -BU5 bundles with AXIe chassis

Table 50. Physical dimensions and power for M8050A bundles with AXIe chassis.

Parameter	
Form factor	Modules are pre-installed in M9505A 5-slot AXIe chassis
Physical dimensions (W x H x D)	Depth including semi-rigid cables without remote heads: M8050A-BU2 / -BU3: 462 mm x 193 mm x 485 mm M8050A-BU4 / -BU5: 462 mm x 384 mm x 485 mm
Weight net	Without modules, without packaging material, without filler panels: M8050A-BU2: 13.3 kg (M9505A) M8050A-BU3: 2.9 kg (M9537A) +13.3 kg (M9505A) M8050A-BU4: 26.6 kg (2 x M9505A) M8050A-BU5: 2.9 kg (M9537A) + 26.6 kg (2 x M9505A)
Weight shipping	Weight per system package only (wo chassis, wo modules) M8050A-BU2 / -BU3: 12.3 kg M8050A-BU4 / -BU5: 24.6 kg (2 x M8050A-BU2)

Specification Definitions

If not otherwise stated all outputs need to be terminated with 50 Ω to GND.

All M8042A specifications if not otherwise stated are valid after the remote heads and at the end of the matched reference cable pair. The reference cable is M8058A-801 when used with M8058A/ M8068A remote head and cable M8059A-801 when used with the M8059A/ M8069A remote head.

All M8043A specifications if not otherwise stated are valid using the recommended cable pair M8058A-801 (length 150 mm,1.85 mm, matched cable pair).

Specification (spec.)

The warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0 °C to 40 °C and a 15-minute warm up period. Within ±10 °C after auto calibration. All specifications include measurement uncertainty and were created in compliance with ISO-17025 methods. Data published in this document are specifications (spec) only where specifically indicated.

Typical (typ.)

The characteristic performance, which 80% or more of manufactured instruments will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 23 °C).

Nominal (nom.)

The mean or average characteristic performance, or the value of an attribute that is determined by design such as a connector type, physical dimension, or operating speed. This data is not warranted and is measured at room temperature (approximately 23 °C).

Measured (meas.)

An attribute measured during development for purposes of communicating the expected performance. This data is not warranted and is measured at room temperature (approximately 23 °C).

Accuracy

Represents the traceable accuracy of a specified parameter. Includes measurement error and time base error, and calibration source uncertainty.

Related Keysight Literature

Description	Pub number
M8050A high-performance BERT 120 GBd - configuration guide	3122-1285.EN
M8040A high-performance BERT 64 GBd - data sheet	5992-1525EN
M8053A interference source 64 GHz – data sheet	3124-1184.EN
M8054A interference source 32 GHz - data sheet	5992-3917EN
M8049A ISI channel boards - data sheet	5992-3617EN
M8067A ISI channel boards – data sheet	3122-2261.EN
M9505A AXIe chassis 5-slot - data sheet	5990-6584EN
M8047B Redriver - data sheet	3122-1648.EN
M8047C Redriver for 32 GBd – data sheet	3124-1732.EN
N7718C Optical reference transmitter – data sheet	3124-1652EN
N5991 Receiver compliance test automation platform - data sheet	5992-4365EN
M8091CKCA Receiver test application for IEEE802.3ck - data sheet	3122-2122.EN
N4917DJCA 1.6T Optical receiver test application software – data sheet	3124-1643.EN
BER measurements using a real-time oscilloscope controlled from M8070B system software – application note	5992-2676EN
Advanced modulation and coding challenges – white paper	5992-3021EN
Equalization: the correction and analysis of degraded signals – white paper	5989-3777EN
Error analysis of PAM4 signals – application note	5992-3268EN
Go to Market with 1.6T - poster	3123-1060EN
Conformance testing of 800G Ethernet links for data center 100G/lane test solution – application note	3121-1220.EN

Keysight Support Services

Accelerate your learning curve, enhance your test uptime, and confidently guarantee your instrument accuracy with Keysight Support Services. Keysight Services are here to support your test needs with expert technical support, instrument repair and calibration, training, alternative acquisition program options, and more.

A KeysightCare agreement provides dedicated, proactive support through a single point of contact for an extensive group of instruments, software, and solutions to ensure optimal uptime, with fast response times and resolution. Explore the services that are right for you.

Keysight Services

Offering	Benefits
KeysightCare 	KeysightCare provides elevated support for Keysight instruments and software, with access to technical support experts who respond within a specified time and ensure committed repair and calibration turnaround times (TAT). KeysightCare offers multiple service agreement tiers, including KeysightCare Assured, Enhanced, and Application Software Support. See the KeysightCare data sheet for details.
KeysightCare Assured	KeysightCare Assured provides a commitment to respond to your engineer's technical needs quickly. When unexpected repairs are necessary, you can count on a committed repair service turnaround time to get you back up and running.
KeysightCare Enhanced	KeysightCare Enhanced includes all the benefits of KeysightCare Assured plus Keysight's accurate and reliable Calibration Services, accelerated and committed TAT, and technical response.
Keysight Support Portal & Knowledge Center	All KeysightCare tiers include access to the Keysight Support Portal, where you can manage support and service resources related to your assets, such as service requests and status, or browse the Knowledge Center.
Education Services	Build confidence and gain new skills to make accurate measurements, with flexible Education Services developed by Keysight experts. Including Start-up Assistance.
Alternative acquisition options	
KeysightAccess	Reduce budget challenges with a lease-based subscription service that offers low monthly payments, enabling you to get the instruments, software, and technical support you want for your test needs.

Recommended services

Maximize your instrument uptime and confidently make accurate measurements by securing technical support, repair, and calibration services with committed response and turnaround times. High-performance instruments include 1 year of KeysightCare Assured or KeysightCare Warranty Plus. Obtain multi-year KeysightCare upfront to eliminate the need for lengthy and tedious paperwork and yearly requests for maintenance budget. Plus, you benefit from secured service for 2, 3, or 5 years.

Service	Function
KeysightCare Enhanced*	**Includes tech support, warranty and calibration**
R-55B-001-1	KeysightCare Enhanced – Upgrade 1 year
R-55B-001-2	KeysightCare Enhanced – Extend to 2 years
R-55B-001-3	KeysightCare Enhanced – Extend to 3 years (Recommended)
R-55B-001-5	KeysightCare Enhanced – Extend to 5 years (Recommended)
KeysightCare Assured*	**Includes tech support and warranty**
R-55A-001-2	KeysightCare Assured – Extend to 2 years
R-55A-001-3	KeysightCare Assured – Extend to 3 years
R-55A-001-5	KeysightCare Assured – Extend to 5 years
Start-Up Assistance	
PS-S40-01	Included – instrument fundamentals and operations starter
PS-S40-04	Recommended – instrument fundamentals and operations starter
PS-S40-02	Optional, technology & measurement science standard learning

* Limited availability might apply. Please review the service definition tool for model number availability and the datasheet for country availability. Coverage might be limited to KeysightCare Warranty Plus (R-55F-001). If KeysightCare Enhanced is available. R-55B-001-2/3/5 must be ordered with R-55B-001-1.